Cyclone V GX FPGA Development Board

Reference Manual

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Additional Information

1. Overview

This document describes the hardware features of the Cyclone® V GX FPGA development board, including the detailed pin-out and component reference information required to create custom FPGA designs that interface with all components of the board.

General Description

The Cyclone V GX FPGA development board provides a hardware platform for developing and prototyping low-power, high-performance, and logic-intensive designs using Altera's Cyclone V GX FPGA device. The board provides a wide range of peripherals and memory interfaces to facilitate the development of Cyclone V GX designs.

One high-speed mezzanine card (HSMC) connectors are available to add additional functionality via a variety of HSMCs available from Altera® and various partners.

To see a list of the latest HSMCs available or to download a copy of the HSMC specification, refer to the Development Board Daughtercards page of the Altera website.

Design advancements and innovations, such as the PCI Express hard IP, partial reconfiguration, and hard memory controller implementation ensure that designs implemented in the Cyclone V GXs operate faster, with lower power, and have a faster time to market than previous FPGA families.

For more information on the following topics, refer to the respective documents:

- Cyclone V device family, refer to the *Cyclone V Device Handbook*.
- PCI Express MegaCore function, refer to the *PCI Express Compiler User Guide*.
- HSMC Specification, refer to the *High Speed Mezzanine Card (HSMC) Specification*.

Board Component Blocks

The development board features the following major component blocks:

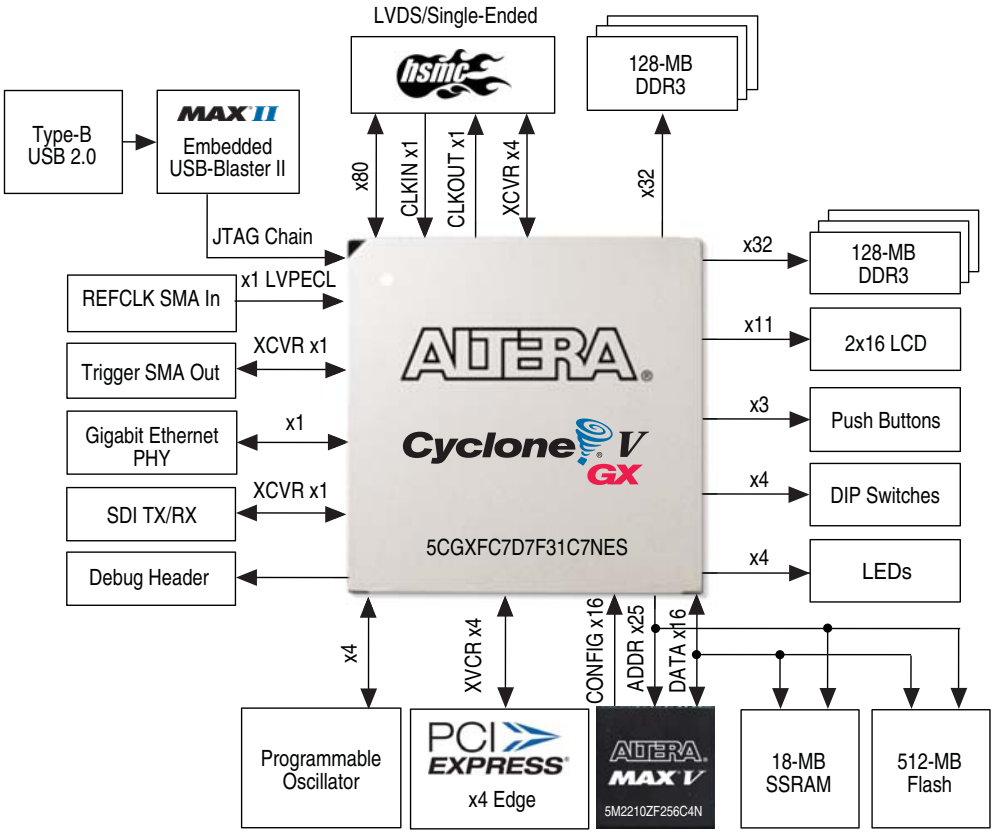
- One Cyclone V GX FPGA (5CGXFC7D6F31C7NES) in a 896-pin FineLine BGA (FBGA) package
  - 150,000 LEs
  - 136,880 adaptive logic modules (ALMs)
  - 7,024 Kbit (Kb) on-die block memory
  - Nine 3.125-Gbps high-speed transceivers
  - Seven fractional phase locked loops (PLLs)
  - 312 18x18-bit multipliers
  - 480 general purpose input/output (GPIO)
  - 1.1-V core voltage
- FPGA configuration circuitry
  - MAX® V CPLD (5M2210ZF256C4N) in a 256-pin FBGA package as the System Controller
  - Flash fast passive parallel (FPP) configuration
  - MAX II CPLD (EPM240M100C4N) in a 100-pin FBGA package as part of the embedded USB-Blaster™ II for use with the Quartus® II Programmer
- Clocking circuitry
  - Programmable clock generator for the FPGA reference clock input
  - 125-MHz LVDS oscillator for the FPGA reference clock input
  - 148.5/148.35-MHz LVDS VCXO for the FPGA reference clock input
  - 50-MHz single-ended oscillator for the FPGA and MAX V CPLD clock input
  - 100-MHz single-ended oscillator for the MAX V CPLD configuration clock input
  - SMA input (LVPECL)
- Memory
  - DDR3 SDRAM
    - Four 128-Mbyte (MB) device with a 16-bit data bus
    - Two 128-MB device with a 8-bit data bus
  - One 18-MB SSRAM
  - One 512-MB synchronous flash

- General user input/output
  - LEDs and displays
    - Four user LEDs
    - One configuration load LED
    - One configuration done LED
    - One error LED
    - Four embedded USB-Blaster II status LEDs
    - Two HSMC interface link LEDs
    - Three PCI Express link width LEDs
    - Five Ethernet LEDs
    - One serial digital interface (SDI) carrier detect LED
    - One power on LED
    - One two-line character LCD display
  - Push buttons
    - One CPU reset push button
    - One MAX V reset push button
    - One program select push button
    - One program configuration push button
    - Three general user push buttons
  - DIP switches
    - Board settings DIP switch
    - JTAG chain control DIP switch
    - PCI Express link width DIP switch
    - General user DIP switch
- Power supply
  - 14–20-V (laptop) DC input
  - PCI Express edge connector
- Mechanical
  - PCI Express card standard size (6.600" x 4.199")

Development Board Block Diagram

Figure 1–1 shows a block diagram of the Cyclone V GX FPGA development board.

Figure 1–1. Cyclone V GX FPGA Development Board Block Diagram



Handling the Board

When handling the board, it is important to observe the following static discharge precaution:

CAUTION

Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

2. Board Components

This chapter introduces the major components on the Cyclone V GX FPGA development board. Figure 2–1 illustrates the component locations and Table 2–1 provides a brief description of all component features of the board.

A complete set of schematics, a physical layout database, and GERBER files for the development board reside in the Cyclone V GX FPGA development kit documents directory.

For information about powering up the board and installing the demonstration software, refer to the *Cyclone V GX FPGA Development Kit User Guide*.

This chapter consists of the following sections:

Board Overview

This section provides an overview of the Cyclone V GX FPGA development board, including an annotated board image and component descriptions. Figure 2–1 shows an overview of the board features.

Figure 2–1. Overview of the Cyclone V GX FPGA Development Board Features

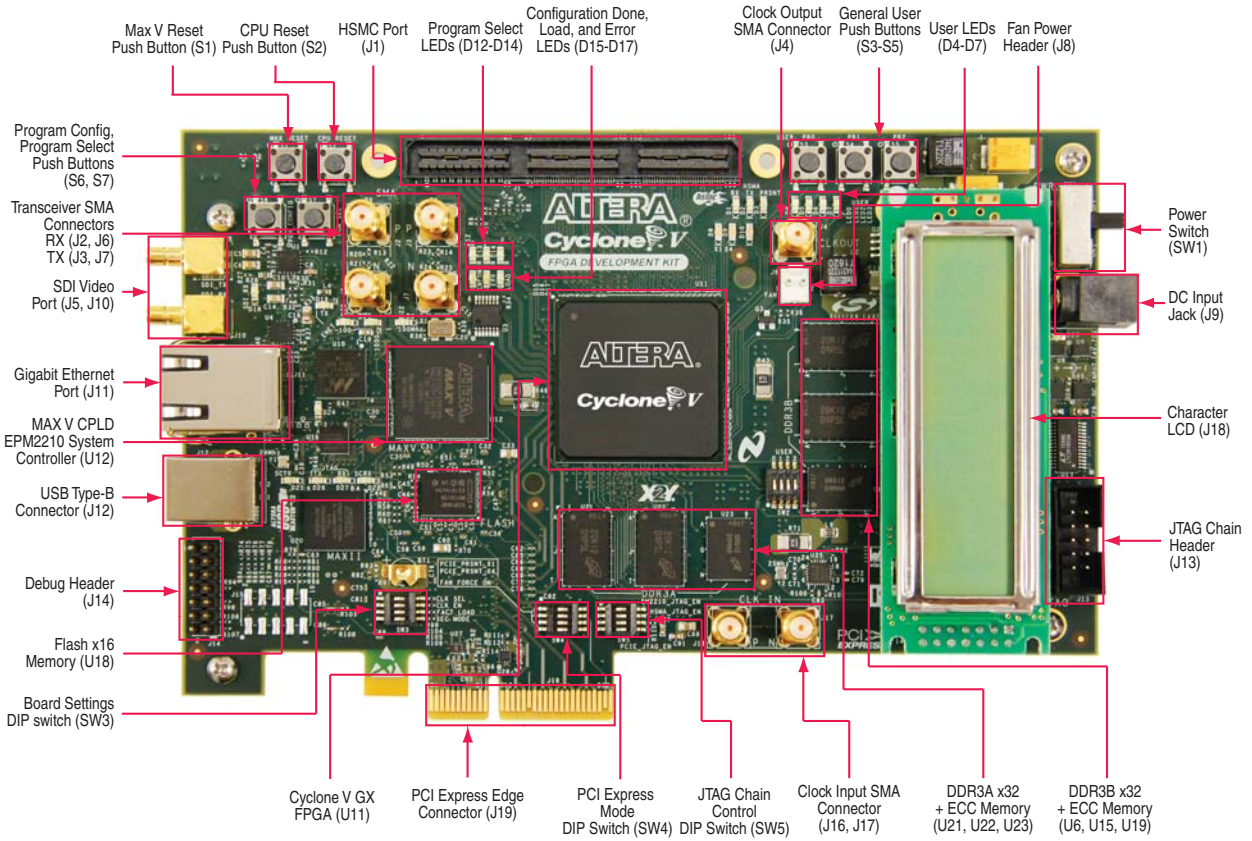


Table 2–1 describes the components and lists their corresponding board references.

Table 2–1. Board Components (Part 1 of 3)

Board Reference	Type	Description
Featured Devices		
U11	FPGA	Cyclone V GX, 5CGXFC7D6F31C7NES, 896-pin FBGA.
U12	CPLD	MAX V CPLD, 5M2210ZF256C4N, 256-pin FBGA.
Configuration, Status, and Setup Elements		
J13	JTAG chain header	Provides access to the JTAG chain and disables the embedded USB-Blaster II when using an external USB-Blaster cable.
SW5	JTAG chain control DIP switch	Remove or include devices in the active JTAG chain.
J12	USB type-B connector	USB interface for FPGA programming and debugging through the embedded USB-Blaster II JTAG via a type-B USB cable.

Table 2–1. Board Components (Part 2 of 3)

Board Reference	Type	Description
SW3	Board settings DIP switch	Controls the MAX V CPLD 5M2210 System Controller functions such as clock enable, SMA clock input control, and which image to load from flash memory at power-up.
SW4	PCI Express DIP switch	Controls the PCI Express lane width by connecting the `prsnt` pins together on the PCI Express edge connector.
S7	Program select push button	Toggles the program select LEDs, which selects the program image that loads from flash memory to the FPGA.
S6	Program configuration push button	Load image from flash memory to the FGPA based on the settings of the program select LEDs.
D15	Configuration done LED	Illuminates when the FPGA is configured.
D17	Load LED	Illuminates when the MAX V CPLD 5M2210 System Controller is actively configuring the FPGA.
D16	Error LED	Illuminates when the FPGA configuration from flash memory fails.
D23	Power LED	Illuminates when 5.0-V power is present.
D12, D13, D14	Program select LEDs	Illuminates to show the LED sequence that determines which flash memory image loads to the FPGA when you press the program select push button. Refer to Table 2–6 for the LED settings.
D19, D20, D21, D22, D24	Ethernet LEDs	Illuminates to show the connection speed as well as transmit or receive activity.
D1, D2	HSMC port LEDs	You can configure these LEDs to indicate transmit or receive activity.
D3	HSMC port present LED	Illuminates when a daughtercard is plugged into the HSMC port A.
D8, D9, D10	PCI Express link LEDs	You can configure these LEDs to indicate the PCI Express link width (x1, x4) and Gen1 link.
Clock Circuitry		
U25	Quad-output oscillator	Programmable oscillator with default frequencies of 125 MHz, 409.6 MHz, 156.25 MHz, and 100 MHz. The frequency is programmable using the clock control GUI running on the MAX V CPLD 5M2210 System Controller.
X2	148.5-MHz oscillator	148.500-MHz voltage controlled crystal oscillator for the serial digital interface (SDI) video. This oscillator is programmable to any frequency between 20–810 MHz using the clock control GUI running on the MAX V CPLD 5M2210 System Controller.
X4	50-MHz oscillator	50.000-MHz crystal oscillator for general purpose logic.
X1	100-MHz oscillator	100.000-MHz crystal oscillator for the MAX V CPLD 5M2210 System Controller.
J2, J3, J6, J7	Transceiver SMA connectors	Drives serial data input/output to or from the SDI video port.
J16, J17	Clock input SMA connectors	Drive LVPECL-compatible clock inputs into the clock multiplexer buffer.
J4	Clock output SMA connector	Drive out 2.5-V CMOS clock output from the FPGA.
General User Input/Output		
D4–D7	User LEDs	Four user LEDs. Illuminates when driven low.
SW2	User DIP switch	Quad user DIP switches. When the switch is ON, a logic 0 is selected.
S2	CPU reset push button	Reset the FPGA logic.

Table 2–1. Board Components (Part 3 of 3)

Board Reference	Type	Description
S1	MAX V reset push button	Reset the MAX V CPLD 5M2210 System Controller.
S3, S4, S5	General user push buttons	Three user push buttons. Driven low when pressed.
Memory Devices		
U6, U15, U21, U22, U19, U23	DDR3 x32 memory	Four 128-MB DDR3 SDRAM with a 16-bit data bus and two 128-MB DDR3 SDRAM with a 8-bit data bus.
U37	SSRAM x16 memory	18-MB standard synchronous RAM with a 12-bit data bus and 4-bit parity.
U18	Flash x16 memory	512-MB synchronous flash devices with a 16-bit data bus for non-volatile memory.
Communication Ports		
J19	PCI Express edge connector	Gold-plated edge fingers connector for up to ×8 signaling in Gen1 mode.
J1	HSMC port	Provides eight transceiver channels and 84 CMOS or 17 LVDS channels per the HSMC specification.
J11	Gigabit Ethernet port	RJ-45 connector which provides a 10/100/1000 Ethernet connection via a Marvell 88E1111 PHY and the FPGA-based Altera Triple Speed Ethernet MegaCore function in RGMII mode.
Video and Display Ports		
J18	Character LCD	Connector that interfaces to a provided 16 character × 2 line LCD module along with two standoffs.
J5, J10	SDI video port	Two 75-Ω sub-miniature version B (SMB) connectors that provide a full-duplex SDI interface through a LMH0303 cable driver and LMH0384 cable equalizer.
Power Supply		
J19	PCI Express edge connector	Interfaces to a PCI Express root port such as an appropriate PC motherboard.
J9	DC input jack	Accepts a 14–20-V DC power supply. Do not use this input jack while the board is plugged into a PCI Express slot.
SW1	Power switch	Switch to power on or off the board when power is supplied from the DC input jack.

Featured Device: Cyclone V GX FPGA

The Cyclone V GX FPGA development board features a Cyclone V GX 5CGXFC7D6F31C7NES device (U11) in a 896-pin FBGA package.

For more information about Cyclone V device family, refer to the *Cyclone V Device Handbook*.

Table 2–2 describes the features of the Cyclone V GX 5CGXFC7D6F31C7NES device.

Table 2–2. Cyclone V GX FPGA Features

ALMs	Equivalent LEs	M10K RAM Blocks	Total RAM (Kbits)	18-bit × 18-bit Multipliers	PLLs	Transceivers	Package Type
136,880	150,000	1,726	7,024	312	7	9	896-pin FBGA

I/O Resources

The Cyclone V GX 5CGXFC7D6F31C7NES device has total of 480 user I/Os and nine transceiver channels. Table 2–3 lists the Cyclone V GX device I/O pin count and usage by function on the board.

Table 2–3. Cyclone V GX Device I/O Pin Count

Function	I/O Standard	I/O Count	Special Pins
DDR3A	1.5-V SSTL	81	One differential x4 DQS pin
DDR3B	1.5-V SSTL	81	One differential x4 DQS pin
Flash, SSRAM, and MAX V FSM bus	2.5-V CMOS	80	—
PCI Express x4 port	2.5-V CMOS + XCVR	13	One reference clock
HSMA port	2.5-V CMOS + LVDS + XCVR	93	Four transceivers, 17 LVDS, I²C
Gigabit Ethernet port	2.5-V CMOS + LVDS	6	—
Embedded USB-Blaster II	2.5-V CMOS	19	—
SDI video port	2.5-V CMOS + XCVR	6	One reference clock
Push buttons	2.5-V CMOS	4	One `DEV_CLRn` pin
DIP switches	2.5-V CMOS	4	—
Character LCD	2.5-V CMOS	11	—
LEDs	2.5-V CMOS	7	—
Clock or Oscillators	2.5-V CMOS + LVDS + PCML	18	Nine reference clock
Total I/O Used:		**423**	

MAX V CPLD 5M2210 System Controller

The board utilizes the 5M2210 System Controller, an Altera MAX V CPLD, for the following purposes:

- FPGA configuration from flash
- Power measurement
- Control and status registers for remote system update

Figure 2–2 illustrates the MAX V CPLD 5M2210 System Controller's functionality and external circuit connections as a block diagram.

Figure 2–2. MAX V CPLD 5M2210 System Controller Block Diagram

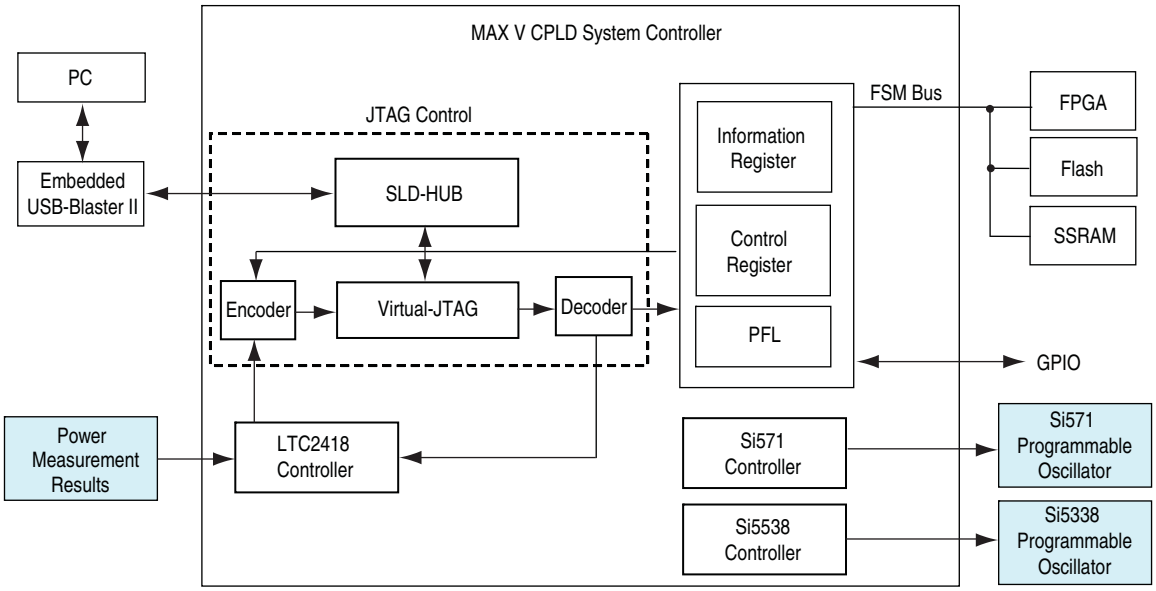


Table 2–4 lists the I/O signals present on the MAX V CPLD 5M2210 System Controller. The signal names and functions are relative to the MAX V device.

Table 2–4. MAX V CPLD 5M2210 System Controller Device Pin-Out (Part 1 of 5)

Board Reference (U12)	Schematic Signal Name	I/O Standard	Description
N4	5M2210_JTAG_TMS	2.5-V	MAX V JTAG TMS
E13	CLK50_EN	2.5-V	50 MHz oscillator enable
J5	CLK_CONFIG	2.5-V	100 MHz configuration clock input
N14	CLK_ENABLE	2.5-V	DIP switch for clock oscillator enable
N15	CLK_SEL	2.5-V	DIP switch for clock select—SMA or oscillator
J12	CLKIN_50_MAXV	2.5-V	50 MHz clock input
L5	CLOCK_SCL	2.5-V	Programmable oscillator I2C clock
K4	CLOCK_SDA	2.5-V	Programmable oscillator I2C data
R7	CPU_RESETN	2.5-V	FPGA reset push button
M16	EXTRA_SIG0	2.5-V	Embedded USB-Blaster II interface. Reserved for future use

Table 2–4. MAX V CPLD 5M2210 System Controller Device Pin-Out (Part 2 of 5)

Board Reference (U12)	Schematic Signal Name	I/O Standard	Description
P9	EXTRA_SIG1	2.5-V	Embedded USB-Blaster II interface. Reserved for future use
M8	EXTRA_SIG2	2.5-V	Embedded USB-Blaster II interface. Reserved for future use
P15	FACTORY_LOAD	2.5-V	DIP switch to load factory or user design at power-up
R14	FACTORY_REQUEST	2.5-V	Embedded USB-Blaster II request to send FACTORY command
N12	FACTORY_STATUS	2.5-V	Embedded USB-Blaster II FACTORY command status
E12	FAN_FORCE_ON	2.5-V	DIP switch to on or off the fan
T5	FLASH_ADVN	2.5-V	FSM bus flash memory address valid
P7	FLASH_CEN	2.5-V	FSM bus flash memory chip enable
M6	FLASH_CLK	2.5-V	FSM bus flash memory clock
N6	FLASH_OEN	2.5-V	FSM bus flash memory output enable
N7	FLASH_RDYBSYN	2.5-V	FSM bus flash memory ready
R6	FLASH_RESETN	2.5-V	FSM bus flash memory reset
R5	FLASH_WEN	2.5-V	FSM bus flash memory write enable
H13	FPGA_CONF_DONE	2.5-V	FPGA configuration done LED
H16	FPGA_CONFIG_D0	2.5-V	FPGA configuration data
G15	FPGA_CONFIG_D1	2.5-V	FPGA configuration data
H15	FPGA_CONFIG_D2	2.5-V	FPGA configuration data
C15	FPGA_CONFIG_D3	2.5-V	FPGA configuration data
E16	FPGA_CONFIG_D4	2.5-V	FPGA configuration data
D16	FPGA_CONFIG_D5	2.5-V	FPGA configuration data
F14	FPGA_CONFIG_D6	2.5-V	FPGA configuration data
E15	FPGA_CONFIG_D7	2.5-V	FPGA configuration data
G13	FPGA_CONFIG_D8	2.5-V	FPGA configuration data
H14	FPGA_CONFIG_D9	2.5-V	FPGA configuration data
D15	FPGA_CONFIG_D10	2.5-V	FPGA configuration data
G16	FPGA_CONFIG_D11	2.5-V	FPGA configuration data
F16	FPGA_CONFIG_D12	2.5-V	FPGA configuration data
E14	FPGA_CONFIG_D13	2.5-V	FPGA configuration data
J13	FPGA_CONFIG_D14	2.5-V	FPGA configuration data
F15	FPGA_CONFIG_D15	2.5-V	FPGA configuration data
M13	FPGA_CVP_CONFDONE	2.5-V	FPGA configuration via protocol done LED
P4	FPGA_DCLK	2.5-V	FPGA configuration clock
L14	FPGA_NCONFIG	2.5-V	FPGA configuration active
P5	FPGA_NSTATUS	2.5-V	FPGA configuration ready
J14	FPGA_PR_DONE	2.5-V	FPGA partial reconfiguration done
M15	FPGA_PR_ERROR	2.5-V	FPGA partial reconfiguration error
D13	FPGA_PR_READY	2.5-V	FPGA partial reconfiguration ready
F13	FPGA_PR_REQUEST	2.5-V	FPGA partial reconfiguration request

Table 2–4. MAX V CPLD 5M2210 System Controller Device Pin-Out (Part 3 of 5)

Board Reference (U12)	Schematic Signal Name	I/O Standard	Description
J4	FSM_A0	2.5-V	FSM address bus
G5	FSM_A1	2.5-V	FSM address bus
F5	FSM_A2	2.5-V	FSM address bus
F6	FSM_A3	2.5-V	FSM address bus
E5	FSM_A4	2.5-V	FSM address bus
D1	FSM_A5	2.5-V	FSM address bus
D2	FSM_A6	2.5-V	FSM address bus
E1	FSM_A7	2.5-V	FSM address bus
E2	FSM_A8	2.5-V	FSM address bus
E4	FSM_A9	2.5-V	FSM address bus
H4	FSM_A10	2.5-V	FSM address bus
F1	FSM_A11	2.5-V	FSM address bus
F2	FSM_A12	2.5-V	FSM address bus
G3	FSM_A13	2.5-V	FSM address bus
G2	FSM_A14	2.5-V	FSM address bus
J2	FSM_A15	2.5-V	FSM address bus
J3	FSM_A16	2.5-V	FSM address bus
G1	FSM_A17	2.5-V	FSM address bus
F3	FSM_A18	2.5-V	FSM address bus
D3	FSM_A19	2.5-V	FSM address bus
C3	FSM_A20	2.5-V	FSM address bus
G4	FSM_A21	2.5-V	FSM address bus
F4	FSM_A22	2.5-V	FSM address bus
E3	FSM_A23	2.5-V	FSM address bus
C2	FSM_A24	2.5-V	FSM address bus
H2	FSM_A25	2.5-V	FSM address bus
H3	FSM_A26	2.5-V	FSM address bus
R3	FSM_D0	2.5-V	FSM data bus
T2	FSM_D1	2.5-V	FSM data bus
K1	FSM_D2	2.5-V	FSM data bus
L1	FSM_D3	2.5-V	FSM data bus
K3	FSM_D4	2.5-V	FSM data bus
K2	FSM_D5	2.5-V	FSM data bus
M2	FSM_D6	2.5-V	FSM data bus
L2	FSM_D7	2.5-V	FSM data bus
M3	FSM_D8	2.5-V	FSM data bus
M1	FSM_D9	2.5-V	FSM data bus
N1	FSM_D10	2.5-V	FSM data bus
N3	FSM_D11	2.5-V	FSM data bus

Table 2–4. MAX V CPLD 5M2210 System Controller Device Pin-Out (Part 4 of 5)

Board Reference (U12)	Schematic Signal Name	I/O Standard	Description
N2	FSM_D12	2.5-V	FSM data bus
L3	FSM_D13	2.5-V	FSM data bus
R1	FSM_D14	2.5-V	FSM data bus
P2	FSM_D15	2.5-V	FSM data bus
L15	HSMA_PRSNTN	2.5-V	HSMC port A present
L6	JTAG_5M2210_TDI	2.5-V	MAX V CPLD JTAG chain data in
M5	JTAG_5M2210_TDO	2.5-V	MAX V CPLD JTAG chain data out
P3	JTAG_TCK	2.5-V	JTAG chain clock
P11	M570_CLOCK	2.5-V	25-MHz clock to embedded USB-Blaster II for sending FACTORY command
P12	M570_PCIE_JTAG_EN	2.5-V	Low signal to disable the embedded USB-Blaster II when PCI Express is the master to the JTAG chain
B10	MAX5_BEN0	2.5-V	FSM bus MAX V byte enable 0
A9	MAX5_BEN1	2.5-V	FSM bus MAX V byte enable 1
C11	MAX5_BEN2	2.5-V	FSM bus MAX V byte enable 2
C10	MAX5_BEN3	2.5-V	FSM bus MAX V byte enable 3
P8	MAX5_CLK	2.5-V	FSM bus MAX V clock
B12	MAX5_CSN	2.5-V	FSM bus MAX V chip select
C12	MAX5_OEN	2.5-V	FSM bus MAX V output enable
A10	MAX5_WEN	2.5-V	FSM bus MAX V write enable
L13	MAX_CONF_DONEN	2.5-V	Embedded USB-Blaster II configuration done LED
P14	MAX_ERROR	2.5-V	FPGA configuration error LED
D14	MAX_LOAD	2.5-V	FPGA configuration active LED
M9	MAX_RESETN	2.5-V	MAX V reset push button
F11	MSEL0	2.5-V	FPGA mode select 0
F12	MSEL1	2.5-V	FPGA mode select 1
K12	MSEL2	2.5-V	FPGA mode select 2
M14	MSEL3	2.5-V	FPGA mode select 3
N13	MSEL4	2.5-V	FPGA mode select 4
J15	OVERTEMP	2.5-V	Temperature monitor fan enable
M7	PCIE_JTAG_EN	2.5-V	DIP switch to enable the PCI Express JTAG master
L12	PGM_CONFIG	2.5-V	Load the flash memory image identified by the PGM LEDs
M4	PGM_LED0	2.5-V	Flash memory PGM select indicator 0
K13	PGM_LED1	2.5-V	Flash memory PGM select indicator 1
L11	PGM_LED2	2.5-V	Flash memory PGM select indicator 2
L4	PGM_SEL	2.5-V	Toggles the PGM_LED[2:0] LED sequence
K14	SDI_FAULT	2.5-V	SDI data transmission fault
N5	SDI_RX_BYPASS	2.5-V	SDI equalization bypass
P6	SDI_RX_EN	2.5-V	SDI receive enable

Table 2–4. MAX V CPLD 5M2210 System Controller Device Pin-Out (Part 5 of 5)

Board Reference (U12)	Schematic Signal Name	I/O Standard	Description
K5	SDI_SCL	2.5-V	SDI clock
L16	SDI_SDA	2.5-V	SDI data
N16	SDI_TX_EN	2.5-V	SDI transmit enable
R12	SECURITY_MODE	2.5-V	DIP switch for the embedded USB-Blaster II to send FACTORY command at power up
K16	SENSE_CS0N	2.5-V	Power monitor chip select
H1	SENSE_SCK	2.5-V	Power monitor SPI clock
G12	SENSE_SDI	2.5-V	Power monitor SPI data in
C14	SENSE_SDO	2.5-V	Power monitor SPI data out
J1	SI571_EN	2.5-V	Si571 programmable VCXO enable
R8	USB_CFG0	2.5-V	Embedded USB-Blaster II interface. Reserved for future use
T7	USB_CFG1	2.5-V	Embedded USB-Blaster II interface. Reserved for future use
R4	USB_CFG2	2.5-V	Embedded USB-Blaster II interface. Reserved for future use
R9	USB_CFG3	2.5-V	Embedded USB-Blaster II interface. Reserved for future use
T11	USB_CFG4	2.5-V	Embedded USB-Blaster II interface. Reserved for future use
T15	USB_CFG5	2.5-V	Embedded USB-Blaster II interface. Reserved for future use
T13	USB_CFG6	2.5-V	Embedded USB-Blaster II interface. Reserved for future use
T9	USB_CFG7	2.5-V	Embedded USB-Blaster II interface. Reserved for future use
T10	USB_CFG8	2.5-V	Embedded USB-Blaster II interface. Reserved for future use
T4	USB_CFG9	2.5-V	Embedded USB-Blaster II interface. Reserved for future use
T8	USB_CFG10	2.5-V	Embedded USB-Blaster II interface. Reserved for future use
T12	USB_CFG11	2.5-V	Embedded USB-Blaster II interface. Reserved for future use
H5	USB_CLK	2.5-V	Embedded USB-Blaster II interface clock

FPGA Configuration

This section describes the FPGA, flash memory, and MAX V CPLD 5M2210 System Controller device programming methods supported by the Cyclone V GX FPGA development board.

The Cyclone V GX development board supports the following three configuration methods:

- Embedded USB-Blaster is the default method for configuring the FPGA using the Quartus II Programmer in JTAG mode with the supplied USB cable.
- Flash memory download for configuring the FPGA using stored images from the flash memory on either power-up or pressing the program configuration push button (S6).
- External USB-Blaster for configuring the FPGA using an external USB-Blaster that connects to the JTAG chain header (J13).

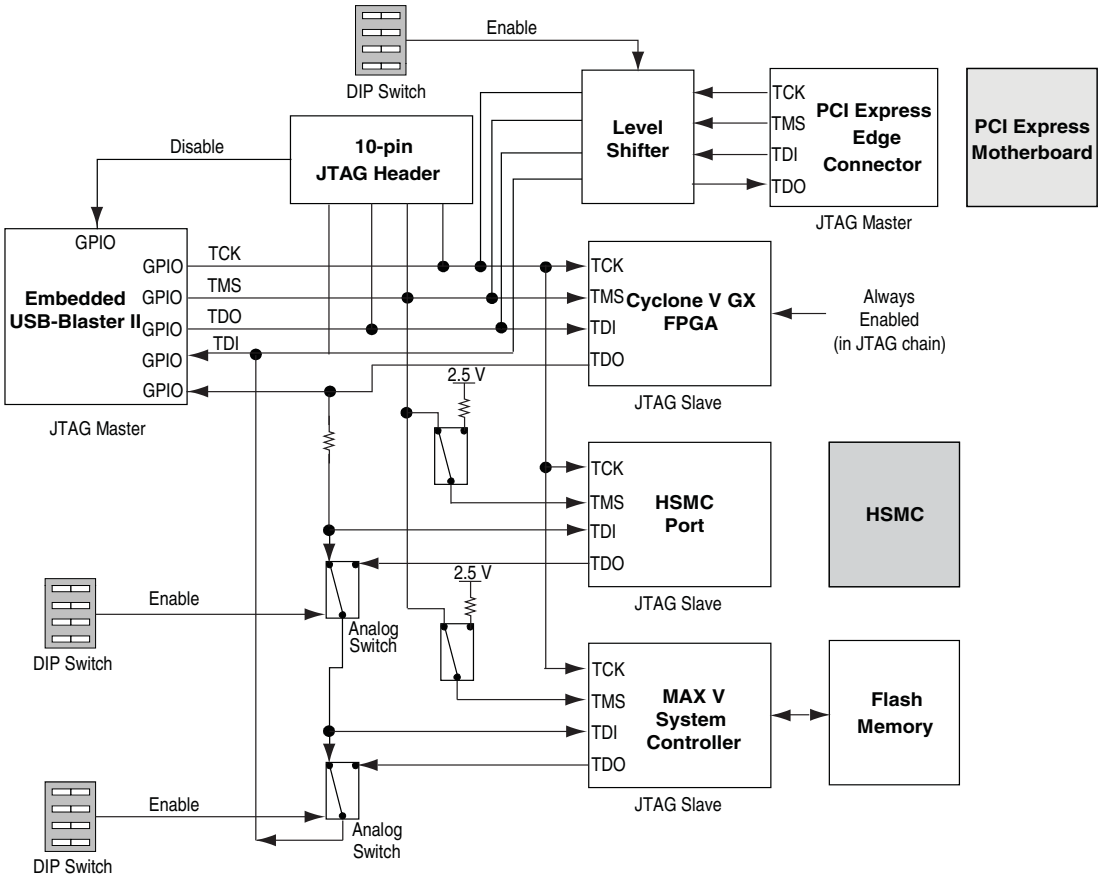
FPGA Programming over Embedded USB-Blaster

This configuration method implements a USB type-B connector (J12), a USB 2.0 PHY device (U16), and an Altera MAX II CPLD EPM240M100C4N (U20) to allow FPGA configuration using a USB cable. This USB cable connects directly between the USB type-B connector on the board and a USB port of a PC running the Quartus II software.

The embedded USB-Blaster in the MAX II CPLD EPM570F100C5N normally masters the JTAG chain.

Figure 2–3 illustrates the JTAG chain.

Figure 2–3. JTAG Chain



The JTAG chain control DIP switch (SW5) controls the jumpers shown in Figure 2–3. To connect a device or interface in the chain, their corresponding switch must be in the OFF position. Slide all the switches in the ON position to only have the FPGA in the chain.

The MAX V CPLD 5M2210 System Controller must be in the JTAG chain to use some of the GUI interfaces.

Table 2–5 lists the USB 2.0 PHY schematic signal names and their corresponding Cyclone V GX device pin numbers.

Table 2–5. USB 2.0 PHY Schematic Signal Names and Functions (Part 1 of 2)

Board Reference (U16)	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
C1	24M_XTALIN	—	3.3-V	Crystal oscillator input
C2	24M_XTALOUT	—	3.3-V	Crystal oscillator output
E1	FX2_D_N	—	3.3-V	USB 2.0 PHY data
E2	FX2_D_P	—	3.3-V	USB 2.0 PHY data
H7	FX2_FLAGA	—	3.3-V	Slave FIFO output status
G7	FX2_FLAGB	—	3.3-V	Slave FIFO output status
H8	FX2_FLAGC	—	3.3-V	Slave FIFO output status
G6	FX2_PA1	—	3.3-V	USB 2.0 PHY port A interface
F8	FX2_PA2	—	3.3-V	USB 2.0 PHY port A interface
F7	FX2_PA3	—	3.3-V	USB 2.0 PHY port A interface
F6	FX2_PA4	—	3.3-V	USB 2.0 PHY port A interface
C8	FX2_PA5	—	3.3-V	USB 2.0 PHY port A interface
C7	FX2_PA6	—	3.3-V	USB 2.0 PHY port A interface
C6	FX2_PA7	—	3.3-V	USB 2.0 PHY port A interface
H3	FX2_PB0	—	3.3-V	USB 2.0 PHY port B interface
F4	FX2_PB1	—	3.3-V	USB 2.0 PHY port B interface
H4	FX2_PB2	—	3.3-V	USB 2.0 PHY port B interface
G4	FX2_PB3	—	3.3-V	USB 2.0 PHY port B interface
H5	FX2_PB4	—	3.3-V	USB 2.0 PHY port B interface
G5	FX2_PB5	—	3.3-V	USB 2.0 PHY port B interface
F5	FX2_PB6	—	3.3-V	USB 2.0 PHY port B interface
H6	FX2_PB7	—	3.3-V	USB 2.0 PHY port B interface
A8	FX2_PD0	—	3.3-V	USB 2.0 PHY port D interface
A7	FX2_PD1	—	3.3-V	USB 2.0 PHY port D interface
B6	FX2_PD2	—	3.3-V	USB 2.0 PHY port D interface
A6	FX2_PD3	—	3.3-V	USB 2.0 PHY port D interface
B3	FX2_PD4	—	3.3-V	USB 2.0 PHY port D interface
A3	FX2_PD5	—	3.3-V	USB 2.0 PHY port D interface
C3	FX2_PD6	—	3.3-V	USB 2.0 PHY port D interface
A2	FX2_PD7	—	3.3-V	USB 2.0 PHY port D interface
B8	FX2_RESETN	V21	3.3-V	Embedded USB-Blaster hard reset
F3	FX2_SCL	—	3.3-V	USB 2.0 PHY serial clock
G3	FX2_SDA	—	3.3-V	USB 2.0 PHY serial data
A1	FX2_SLRDN	—	3.3-V	Read strobe for slave FIFO
B1	FX2_SLWRN	—	3.3-V	Write strobe for slave FIFO

Table 2–5. USB 2.0 PHY Schematic Signal Names and Functions (Part 2 of 2)

Board Reference (U16)	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
B7	FX2_WAKEUP	—	3.3-V	USB 2.0 PHY wake signal
G2	USB_CLK	AA23	3.3-V	USB 2.0 PHY 48-MHz interface clock

FPGA Programming from Flash Memory

Flash memory programming is possible through a variety of methods. The default method is to use the factory design—Board Update Portal. This design is an embedded webserver, which serves the Board Update Portal web page. The web page allows you to select new FPGA designs including hardware, software, or both in an industry-standard S-Record File (**.flash**) and write the design to the user hardware page (page 1) of the flash memory over the network.

The secondary method is to use the pre-built parallel flash loader (PFL) design included in the development kit. The development board implements the Altera PFL megafunction for flash memory programming. The PFL megafunction is a block of logic that is programmed into an Altera programmable logic device (FPGA or CPLD). The PFL functions as a utility for writing to a compatible flash memory device. This pre-built design contains the PFL megafunction that allows you to write either page 0, page 1, or other areas of flash memory over the USB interface using the Quartus II software. This method is used to restore the development board to its factory default settings.

Other methods to program the flash memory can be used as well, including the Nios® II processor.

For more information on the Nios II processor, refer to the Nios II Processor page of the Altera website.

On either power-up or by pressing the program configuration push button, PGM_CONFIG (S6), the MAX V CPLD 5M2210 System Controller's PFL configures the FPGA from the flash memory. The PFL megafunction reads 16-bit data from the flash memory and converts it to fast passive parallel (FPP) format. This 16-bit data is then written to the dedicated configuration pins in the FPGA during configuration.

Pressing the PGM_CONFIG push button (S6) loads the FPGA with a hardware page based on which PGM_LED[2:0] (D11, D12, D13) illuminates. Table 2–6 defines the design that loads when you press the PGM_CONFIG push button.

Table 2–6. PGM_LED Settings (1)

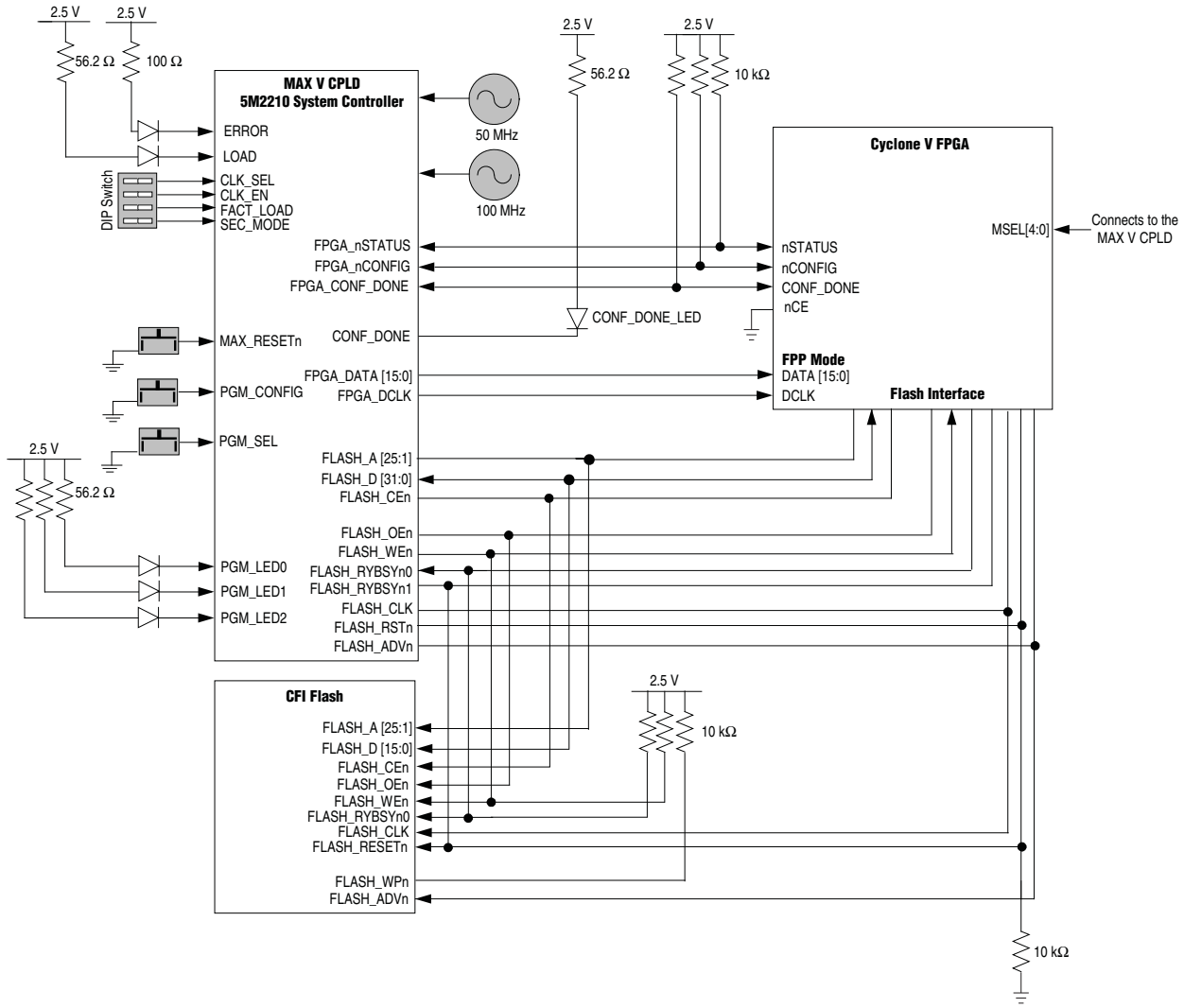
PGM_LED0 (D12)	PGM_LED1 (D13)	PGM_LED2 (D14)	Design
ON	OFF	OFF	Factory hardware
OFF	ON	OFF	User hardware 1
OFF	OFF	ON	User hardware 2

Note to Table 2–6:

(1) ON indicates a setting of '0' while OFF indicates a setting of '1'.

Figure 2–4 shows the PFL configuration.

Figure 2–4. PFL Configuration



For more information on the following topics, refer to the respective documents:

- Board Update Portal, PFL design, and flash memory map storage, refer to the *Cyclone V GX FPGA Development Kit User Guide*.
- PFL megafunction, refer to *Parallel Flash Loader Megafunction User Guide.*

FPGA Programming over External USB-Blaster

The JTAG chain header provides another method for configuring the FPGA using an external USB-Blaster device with the Quartus II Programmer running on a PC. To prevent contention between the JTAG masters, the embedded USB-Blaster is automatically disabled when you connect an external USB-Blaster to the JTAG chain through the JTAG chain header.

Status Elements

The development board includes status LEDs. This section describes the status elements.

Table 2–7 lists the LED board references, names, and functional descriptions.

Table 2–7. Board-Specific LEDs

Board Reference	Schematic Signal Name	I/O Standard	Description
D23	Power	5.0-V	Blue LED. Illuminates when 5.0 V power is active.
D15	MAX_CONF_DONEn	2.5-V	Green LED. Illuminates when the FPGA is successfully configured. Driven by the MAX V CPLD 5M2210 System Controller.
D16	MAX_ERROR	2.5-V	Red LED. Illuminates when the MAX V CPLD 5M2210 System Controller fails to configure the FPGA. Driven by the MAX V CPLD 5M2210 System Controller.
D17	MAX_LOAD	2.5-V	Green LED. Illuminates when the MAX V CPLD 5M2210 System Controller is actively configuring the FPGA. Driven by the MAX V CPLD 5M2210 System Controller.
D12 D13 D14	PGM_LED[0] PGM_LED[1] PGM_LED[2]	2.5-V	Green LEDs. Illuminates to indicate which hardware page loads from flash memory when you press the PGM_SEL push button.
D27, D26 D28, D25	JTAG_RX, JTAG_TX SC_RX, SC_TX	2.5-V	Green LEDs. Illuminates to indicate USB-Blaster II receive and transmit activities.
D19	ENET_LED_TX	2.5-V	Green LED. Illuminates to indicate Ethernet PHY transmit activity. Driven by the Marvell 88E1111 PHY.
D22	ENET_LED_RX	2.5-V	Green LED. Illuminates to indicate Ethernet PHY receive activity. Driven by the Marvell 88E1111 PHY.
D24	ENET_LED_LINK10	2.5-V	Green LED. Illuminates to indicate Ethernet linked at 10 Mbps connection speed. Driven by the Marvell 88E1111 PHY.
D20	ENET_LED_LINK100	2.5-V	Green LED. Illuminates to indicate Ethernet linked at 100 Mbps connection speed. Driven by the Marvell 88E1111 PHY.
D21	ENET_LED_LINK1000	2.5-V	Green LED. Illuminates to indicate Ethernet linked at 1000 Mbps connection speed. Driven by the Marvell 88E1111 PHY.
D18	SDI_RX_CDn	3.3-V	Green LED. Illuminates to indicate that input signal is detected at the SDI RX port. Driven by the SDI cable equalizer.
D3	HSMA_PRSNTn	3.3-V	Green LED. Illuminates when HSMC port A has a board or cable plugged-in such that pin 160 becomes grounded. Driven by the add-in card.

Setup Elements

The development board includes several different kinds of setup elements. This section describes the following setup elements:

- Board settings DIP switch
- JTAG settings DIP switch
- PCI Express control DIP switch
- CPU reset push button
- MAX V reset push button
- Program configuration push button
- Program select push button

Board Settings DIP Switch

The board settings DIP switch (SW3) controls various features specific to the board and the MAX V CPLD 5M2210 System Controller logic design. Table 2–8 lists the switch controls and descriptions.

Table 2–8. Board Settings DIP Switch Controls

Switch	Schematic Signal Name	Description	Default
1	CLK_SEL	ON : Select SMA input clock OFF : Select programmable oscillator clock	OFF
2	CLK_EN	ON : Disable on-board oscillator OFF : Enable on-board oscillator	OFF
3	FACT_LOAD	ON : Load the user design from flash at power up. OFF : Load the factory design from flash at power up.	OFF
4	SEC_MODE	ON : Embedded USB-Blaster II sends FACTORY command at power up. OFF : Embedded USB-Blaster II does not send FACTORY command at power up.	OFF

JTAG Chain Control DIP Switch

The JTAG chain control DIP switch (SW5) either remove or include devices in the active JTAG chain. The Cyclone V GX FPGA is always in the JTAG chain. Table 2–9 lists the switch controls and its descriptions.

Table 2–9. JTAG Chain Control DIP Switch

Switch	Schematic Signal Name	Description	Default
1	5M2210_JTAG_EN	ON : Bypass MAX V CPLD 5M2210 System Controller OFF : MAX V CPLD 5M2210 System Controller in-chain	OFF
2	HSMA_JTAG_EN	ON : Bypass HSMC port A OFF : HSMC port A in-chain	ON

Table 2–9. JTAG Chain Control DIP Switch

Switch	Schematic Signal Name	Description	Default
3	PCIE_JTAG_EN	ON : Bypass PCI Express edge connector OFF : PCI Express edge connector in-chain	ON
4	NC	Not used	—

PCI Express Link Width DIP Switch

The PCI Express link width DIP switch (SW4) enable or disable different link width configurations. Table 2–10 lists the switch controls and descriptions.

Table 2–10. PCI Express Link Width DIP Switch Controls

Switch	Schematic Signal Name	Description	Default
1	PCIE_PRSNT2n_x1	ON : Enable x1 presence detect OFF : Disable x1 presence detect	OFF
2	PCIE_PRSNT2n_x4	ON : Enable x4 presence detect OFF : Disable x4 presence detect	OFF
3	NC	Not used	—
4	FAN_FORCE_ON	ON : Enable fan OFF : Disable fan	OFF

CPU Reset Push Button

The CPU reset push button, CPU_RESETn (S2), is an input to the Cyclone V GX DEV_CLRn pin and is an open-drain I/O from the MAX V CPLD System Controller. This push button is the default reset for both the FPGA and CPLD logic. The MAX V CPLD 5M2210 System Controller also drives this push button during power-on-reset (POR).

MAX V Reset Push Button

The MAX V reset push button, MAX_RESETn (S1), is an input to the MAX V CPLD 5M2210 System Controller. This push button is the default reset for the CPLD logic.

Program Configuration Push Button

The program configuration push button, PGM_CONFIG (S6), is an input to the MAX V CPLD 5M2210 System Controller. This input forces a FPGA reconfiguration from the flash memory. The location in the flash memory is based on the settings of PGM_LED[2:0], which is controlled by the program select push button, PGM_SEL. Valid settings include PGM_LED0, PGM_LED1, or PGM_LED2 on the three pages in flash memory reserved for FPGA designs.

Program Select Push Button

The program select push button, PGM_SEL (S7), is an input to the MAX V CPLD System Controller. This push button toggles the PGM_LED[2:0]sequence that selects which location in the flash memory is used to configure the FPGA. Refer to Table 2–6 for the PGM_LED[2:0] sequence definitions.

Clock Circuitry

This section describes the board's clock inputs and outputs.

On-Board Oscillators

The development board include oscillators with a frequency of 50-MHz, 100-MHz, 148.50-MHz, and a quad-clock programmable oscillator.

Figure 2–5 shows the default frequencies of all external clocks going to the Cyclone V GX FPGA development board.

Figure 2–5. Cyclone V GX FPGA Development Board Clocks

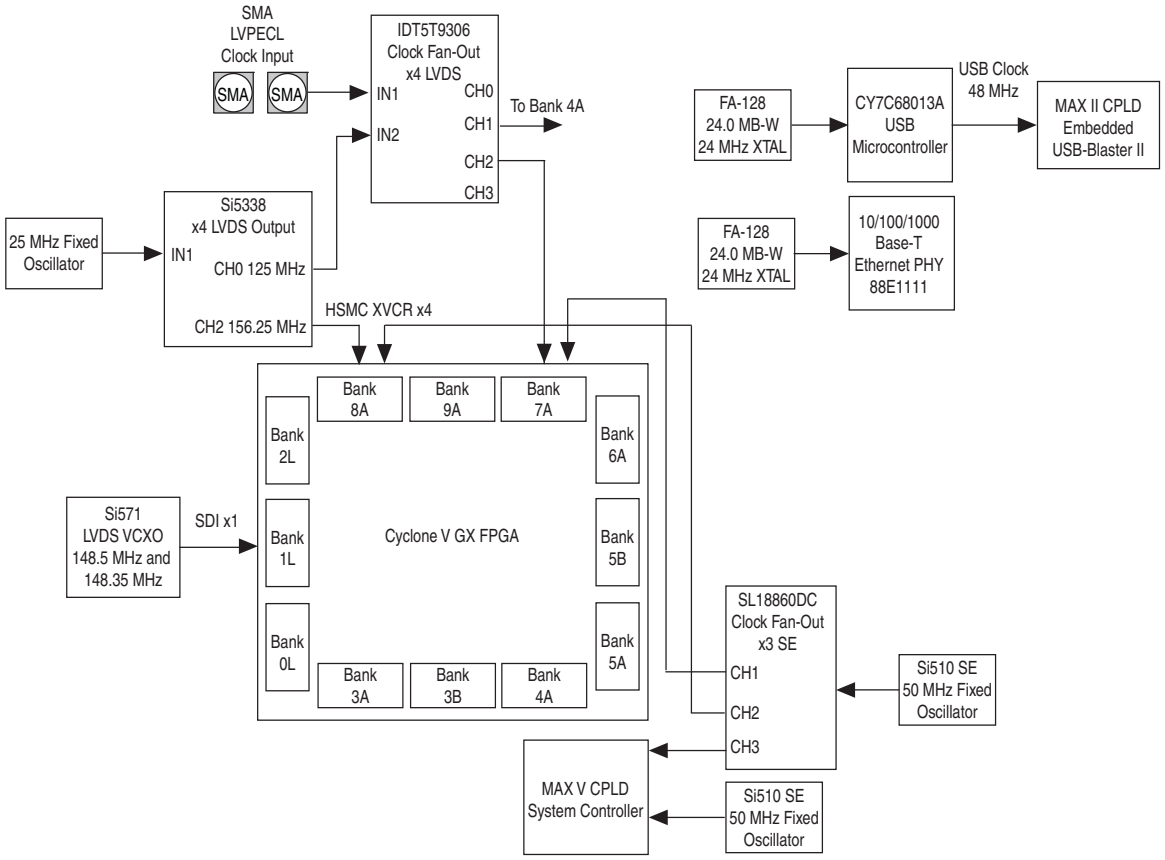


Table 2–11 lists the oscillators, its I/O standard, and voltages required for the development board.

Table 2–11. On-Board Oscillators

Source	Schematic Signal Name	Frequency	I/O Standard	Cyclone V GX Pin Number	Application
X4	CLKIN_50_7A	50.000 MHz	Single-Ended	H17	Top edge
	CLKIN_50_TOP			K15	
X1	CLK_CONFIG	100.000 MHz	2.5V CMOS	—	Fast FPGA configuration
J19	PCIE_REFCLK_P	100.000 MHz	LVDS	W8	PCI Express x4
	PCIE_REFCLK_N			W7	
U25	CLKIN_BANK3B_125_R_P	125.000 MHz	1.5V LVDS (fanout buffer)	Y15	Bottom edge
	CLKIN_BANK3B_125_R_N			AA15	
	CLKIN_BANK4A_125_R_P			AC15	
	CLKIN_BANK4A_125_R_N			AB16	
	REFCLK1_Q2L_P			P8	HSMC port A
	REFCLK1_Q2L_N			N7	
X2	CLK_148_P	148.500 MHz	LVDS	R8	HD-SDI video
	CLK_148_N			R7	

Off-Board Clock Input/Output

The development board has input and output clocks which can be driven onto the board. The output clocks can be programmed to different levels and I/O standards according to the FPGA device's specification.

Table 2–12 lists the clock inputs for the development board.

Table 2–12. Off-Board Clock Inputs

Source	Schematic Signal Name	I/O Standard	Cyclone V GX Pin Number	Description
SMA	CLKIN_SMA_P	LVPECL	—	Input to LVDS fan-out buffer (drives one REFCLK)
	CLKIN_SMA_N	LVPECL	—	
Samtec HSMC	HSMA_CLK_IN0	2.5-V	L15	Single-ended input from the installed HSMC cable or board.
Samtec HSMC	HSMA_CLK_IN_P1	LVDS/2.5-V	H19	LVDS input from the installed HSMC cable or board. Can also support 2x LVTTL inputs.
	HSMA_CLK_IN_N1	LVDS/LVTTL	J18	
Samtec HSMC	HSMA_CLK_IN_P2	LVDS/LVTTL	L14	LVDS input from the installed HSMC cable or board. Can also support 2x LVTTL inputs.
	HSMA_CLK_IN_N2	LVDS/LVTTL	L13	
PCI Express Edge	PCIE_REFCLK_P	LVDS	W8	LVDS input from the PCI Express edge connector.
	PCIE_REFCLK_N	HCSL	W7	

Table 2–13 lists the clock outputs for the development board.

Table 2–13. Off-Board Clock Outputs

Source	Schematic Signal Name	I/O Standard	Cyclone V GX Pin Number	Description
Samtec HSMC	HSMA_CLK_OUT0	2.5V CMOS	J19	FPGA CMOS output (or GPIO)
Samtec HSMC	HSMA_CLK_OUT_P1	LVDS/2.5V CMOS	B26	LVDS output. Can also support 2x CMOS outputs.
	HSMA_CLK_OUT_N1	LVDS/2.5V CMOS	A26	
Samtec HSMC	HSMA_CLK_OUT_P2	LVDS/2.5V CMOS	A25	LVDS output. Can also support 2x CMOS outputs.
	HSMA_CLK_OUT_N2	LVDS/2.5V CMOS	A24	
SMA	CLKOUT_SMA	2.5V CMOS	F9	FPGA CMOS output (or GPIO)

General User Input/Output

This section describes the user I/O interface to the FPGA, including the push buttons, DIP switches, LEDs, and character LCD.

User-Defined Push Buttons

The development board includes three user-defined push buttons. For information on the system and safe reset push buttons, refer to "Setup Elements" on page 2–16.

Board references S3, S4, and S5 are push buttons for controlling the FPGA designs that loads into the Cyclone V GX device. When you press and hold down the switch, the device pin is set to logic 0; when you release the switch, the device pin is set to logic 1. There are no board-specific functions for these general user push buttons.

Table 2–14 lists the user-defined push button schematic signal names and their corresponding Cyclone V GX device pin numbers.

Table 2–14. User-Defined Push Button Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
S3	USER_PB0	AF29	1.5-V	User-defined push buttons
S4	USER_PB1	AF30	1.5-V	
S5	USER_PB2	AE28	1.5-V	

User-Defined DIP Switch

Board reference SW2 is a four-pin DIP switch. This switch is user-defined and provides additional FPGA input control. When the switch is in the OFF position, a logic 1 is selected. When the switch is in the ON position, a logic 0 is selected. There are no board-specific functions for this switch.

Table 2–15 lists the user-defined DIP switch schematic signal names and their corresponding Cyclone V GX device pin numbers.

Table 2–15. User-Defined DIP Switch Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
1	USER_DIPSW0	AG29	1.5-V	User-defined DIP switch that connects to the FPGA
2	USER_DIPSW1	AH29	1.5-V	
3	USER_DIPSW2	AJ29	1.5-V	
4	USER_DIPSW3	AJ28	1.5-V	

User-Defined LEDs

The development board includes general and HSMC user-defined LEDs. This section describes all user-defined LEDs. For information on board specific or status LEDs, refer to "Status Elements" on page 2–15.

General LEDs

Board references D4 through D7 are four user-defined LEDs. The status and debugging signals are driven to the LEDs from the designs loaded into the Cyclone V GX. Driving a logic 0 on the I/O port turns the LED on while driving a logic 1 turns the LED off. There are no board-specific functions for these LEDs.

Table 2–16 lists the general LED schematic signal names and their corresponding Cyclone V GX device pin numbers.

Table 2–16. General LED Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
D4	USER_LED0	AF28	2.5-V	User-defined LEDs
D5	USER_LED1	AG28	2.5-V	
D6	USER_LED2	AH30	2.5-V	
D7	USER_LED3	AJ30	2.5-V	

HSMC LEDs

Board references D1 and D2 are LEDs for the HSMC port. There are no board-specific functions for the HSMC LEDs. The LEDs are labeled TX and RX, and are intended to display data flow to and from the connected daughtercards. The LEDs are driven by the Cyclone V GX device.

Table 2–17 lists the HSMC LED schematic signal names and their corresponding Cyclone V GX device pin numbers.

Table 2–17. HSMC LED Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
D1	HSMA_RX_LED	T11	2.5-V	User-defined LEDs
D2	HSMA_TX_LED	AB26	2.5-V	

PCI Express LEDs

Board references D8 through D10 are PCI Express LEDs for link width indication. There are no board-specific functions for the PCI Express LEDs. You can configure the LEDs to display the functions as listed in Table 2–18. The LEDs are driven by the Cyclone V GX device.

Table 2–18 lists the PCI Express LED schematic signal names and their corresponding Cyclone V GX device pin numbers.

Table 2–18. PCI Express LED Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
D8	PCIE_LED_X1	AD28	2.5-V	Green LED. Configure this LED to display the PCI Express link width x1.
D9	PCIE_LED_X4	AC29	2.5-V	Green LED. Configure this LED to display the PCI Express link width x4.
D10	PCIE_LED_G1	AB28	2.5-V	Green LED. Configure this LED to display the PCI Express Gen1 link.

Character LCD

The development board includes a single 14-pin 0.1" pitch dual-row header that interfaces to a 2 line × 16 character Lumex character LCD. The character LCD has a 14-pin receptacle that mounts directly to the board's 14-pin header, so it can be easily removed for access to components under the display. You can also use the header for debugging or other purposes.

Table 2–19 summarizes the character LCD pin assignments. The signal names and directions are relative to the Cyclone V GX device.

Table 2–19. Character LCD Pin Assignments, Schematic Signal Names, and Functions

Board Reference (J18)	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
7	LCD_DATA0	T10	2.5-V	LCD data bus
8	LCD_DATA1	AH5	2.5-V	LCD data bus
9	LCD_DATA2	AH4	2.5-V	LCD data bus
10	LCD_DATA3	U8	2.5-V	LCD data bus
11	LCD_DATA4	T9	2.5-V	LCD data bus
12	LCD_DATA5	AH6	2.5-V	LCD data bus
13	LCD_DATA6	AG6	2.5-V	LCD data bus
14	LCD_DATA7	R12	2.5-V	LCD data bus
4	LCD_D_Cn	D17	2.5-V	LCD data or command select
5	LCD_WEn	E17	2.5-V	LCD write enable
6	LCD_CSn	C11	2.5-V	LCD chip select

Table 2–20 lists the LCD pin definitions, and is an excerpt from Lumex data sheet.

Table 2–20. LCD Pin Definitions and Functions

Pin Number	Symbol	Level	Function	
1	V_{DD}	—	Power supply	5 V
2	V_{SS}	—		GND (0 V)
3	V_0	—		For LCD drive
4	RS	H/L	Register select signal H: Data input L: Instruction input	
5	R/W	H/L	H: Data read (module to MPU) L: Data write (MPU to module)	
6	E	H, H to L	Enable	
7–14	DB0–DB7	H/L	Data bus—software selectable 4-bit or 8-bit mode	

For more information such as timing, character maps, interface guidelines, and other related documentation, visit www.lumex.com.

Debug Header

This development board includes a 2×7 debug header for debug purposes. The FPGA I/Os route directly to the header for design testing, debugging, or quick verification.

Table 2–21 summarizes the debug header pin assignments, signal names, and functions.

Table 2–21. Debug Header Pin Assignments, Schematic Signal Names, and Functions

Board Reference (J14)	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
1	DEBUG_HDR0	E10	2.5-V	Single-ended signal for debug purposes only
2	DEBUG_HDR6	U22	1.5-V	Single-ended signal for debug purposes only
5	DEBUG_HDR2	L21	1.5-V	Single-ended signal for debug purposes only
8	DEBUG_HDR9	M21	1.5-V	Single-ended signal for debug purposes only
11	SECURITY_CPLD_MRn	—	1.5-V	Test signal

Components and Interfaces

This section describes the development board's communication ports and interface cards relative to the Cyclone V GX device. The development board supports the following communication ports:

- PCI Express
- 10/100/1000 Ethernet
- HSMC
- SDI video output/input

PCI Express

The Cyclone V GX FPGA development board is designed to fit entirely into a PC motherboard with a ×4 PCI Express slot that can accommodate a full height long form factor add-in card. This interface uses the Cyclone V GX's PCI Express hard IP block, saving logic resources for the user logic application. The PCI express edge connector has a presence detect feature to allow the motherboard to determine if a card is installed.

For more information on using the PCI Express hard IP block, refer to the *PCI Express Compiler User Guide*.

The PCI Express interface supports auto-negotiating channel width from ×1 to ×4 by using Altera's PCIe MegaCore IP. You can also configure this board to a ×1 or ×4 interface through a DIP switch that connects the `PRSNTn` pins for each bus width.

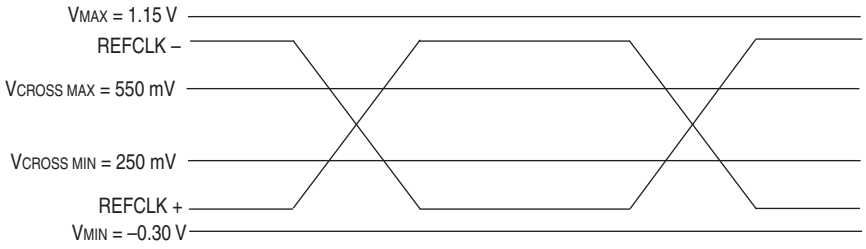
The PCI Express interface has a connection speed of 2.5 Gbps/lane for a maximum of 20 Gbps full-duplex (Gen1).

The power for the board can be sourced entirely from the PCI Express edge connector when installed into a PC motherboard. Although the board can also be powered by a laptop power supply for use on a lab bench, Altera recommends that you do not power up from both supplies at the same time. Ideal diode power sharing devices have been designed into this board to prevent damages or back-current from one supply to the other.

The `PCIE_REFCLK_P/N` signal is a 100 MHz differential input that is driven from the PC motherboard on to this board through the edge connector. This signal connects directly to a Cyclone V GX `REFCLK` input pin pair using DC coupling. This clock is terminated on the motherboard and therefore, no on-board termination is required. This clock can have spread-spectrum properties that change its period between 9.847 ps to 10.203 ps. The I/O standard is High-Speed Current Steering Logic (HCSL).

Figure 2–6 shows the PCI Express reference clock levels.

Figure 2–6. PCI Express Reference Clock Levels



The JTAG and SMB are optional signals in the PCI Express specification. Both types of signals are wired to the Cyclone V GX but are not required for normal operation.

Table 2–22 summarizes the PCI Express pin assignments. The signal names and directions are relative to the Cyclone V GX.

Table 2–22. PCI Express Pin Assignments, Schematic Signal Names, and Functions

Board Reference (J19)	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
A5	PCIE_JTAG_TCK	—	LVTTL	JTAG chain clock
A6	PCIE_JTAG_TDI	—	LVTTL	JTAG chain data in
A7	PCIE_JTAG_TDO	—	LVTTL	JTAG chain data out
A8	PCIE_JTAG_TMS	—	LVTTL	JTAG chain mode select
A11	PCIE_PERSTN	W27	LVTTL	Reset
A1	PCIE_PRSNT1N	—	LVTTL	Link width DIP switch
B17	PCIE_PRSNT2N_X1	—	LVTTL	Hot plug present detect
B31	PCIE_PRSNT2N_X4	—	LVTTL	Hot plug present detect
A13	PCIE_REFCLK_P	W8	HCSL	Reference clock input
A14	PCIE_REFCLK_N	W7	HCSL	Reference clock input
B14	PCIE_RX_P0	AG2	1.5-V PCML	Receive bus
B15	PCIE_RX_N0	AG1	1.5-V PCML	Receive bus
B19	PCIE_RX_P1	AE2	1.5-V PCML	Receive bus
B20	PCIE_RX_N1	AE1	1.5-V PCML	Receive bus
B23	PCIE_RX_P2	AC2	1.5-V PCML	Receive bus
B24	PCIE_RX_N2	AC1	1.5-V PCML	Receive bus
B27	PCIE_RX_P3	AA2	1.5-V PCML	Receive bus
B28	PCIE_RX_N3	AA1	1.5-V PCML	Receive bus
B5	PCIE_SMBCLK	R11	2.5-V	SMB clock
B6	PCIE_SMBDAT	V22	2.5-V	SMB data
A16	PCIE_TX_P0	AF4	1.5-V PCML	Transmit bus
A17	PCIE_TX_N0	AF3	1.5-V PCML	Transmit bus
A21	PCIE_TX_P1	AD4	1.5-V PCML	Transmit bus
A22	PCIE_TX_N1	AD3	1.5-V PCML	Transmit bus

Table 2–22. PCI Express Pin Assignments, Schematic Signal Names, and Functions

Board Reference (J19)	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
A25	PCIE_TX_P2	AB4	1.5-V PCML	Transmit bus
A26	PCIE_TX_N2	AB3	1.5-V PCML	Transmit bus
A29	PCIE_TX_P3	Y4	1.5-V PCML	Transmit bus
A30	PCIE_TX_N3	Y3	1.5-V PCML	Transmit bus
B11	PCIE_WAKEn	Y27	2.5-V	Wake signal

10/100/1000 Ethernet

The development board supports 10/100/1000 base-T Ethernet using an external Marvell 88E1111 PHY and Altera Triple-Speed Ethernet MegaCore MAC function. The PHY-to-MAC interface employs a RGMII interface. The MAC function must be provided in the FPGA for typical networking applications.

The Marvell 88E1111 PHY uses 2.5-V and 1.0-V power rails and requires a 25-MHz reference clock driven from a dedicated oscillator. The PHY interfaces to a RJ45 model with internal magnetics that can be used for driving copper lines with Ethernet traffic.

Figure 2–7 shows the RGMII interface between the FPGA (MAC) and Marvell 88E1111 PHY.

Figure 2–7. RGMII Interface between FPGA (MAC) and Marvell 88E1111 PHY

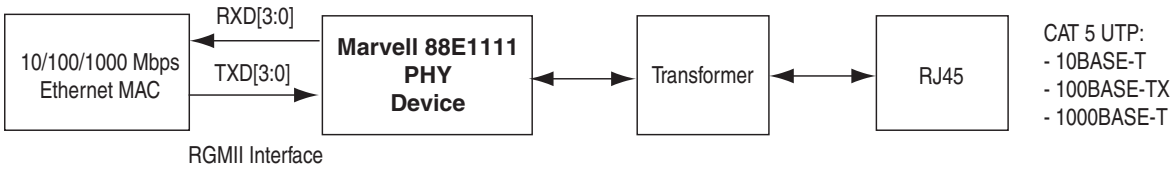


Table 2–23 lists the Ethernet PHY interface pin assignments.

Table 2–23. Ethernet PHY Pin Assignments, Signal Names and Functions (Part 1 of 2)

Board Reference (U10)	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
8	ENET_GTX_CLK	U9	2.5-V CMOS	125-MHz RGMII transmit clock
23	ENET_INTN	B17	2.5-V CMOS	Management bus interrupt
60	ENET_LED_DUPLEX	—	2.5-V CMOS	Duplex or collision LED. Not used
70	ENET_LED_DUPLEX	—	2.5-V CMOS	Duplex or collision LED. Not used
76	ENET_LED_LINK10	—	2.5-V CMOS	10-Mb link LED
74	ENET_LED_LINK100	—	2.5-V CMOS	100-Mb link LED
73	ENET_LED_LINK1000	—	2.5-V CMOS	1000-Mb link LED
58	ENET_LED_RX	—	2.5-V CMOS	RX data active LED
69	ENET_LED_RX	—	2.5-V CMOS	RX data active LED
68	ENET_LED_TX	—	2.5-V CMOS	TX data active LED
25	ENET_MDC	C17	2.5-V CMOS	Management bus data clock

Table 2–23. Ethernet PHY Pin Assignments, Signal Names and Functions (Part 2 of 2)

Board Reference (U10)	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
24	ENET_MDIO	D18	2.5-V CMOS	Management bus data
28	ENET_RESETN	J17	2.5-V CMOS	Device reset
2	ENET_RX_CLK	G17	2.5-V CMOS	RGMII receive clock
95	ENET_RX_D0	AF8	2.5-V CMOS	RGMII receive data bus
92	ENET_RX_D1	AB9	2.5-V CMOS	RGMII receive data bus
93	ENET_RX_D2	AA9	2.5-V CMOS	RGMII receive data bus
91	ENET_RX_D3	AH7	2.5-V CMOS	RGMII receive data bus
94	ENET_RX_DV	D19	2.5-V CMOS	RGMII receive data valid
11	ENET_TX_D0	AG7	2.5-V CMOS	RGMII transmit data bus
12	ENET_TX_D1	AB8	2.5-V CMOS	RGMII transmit data bus
14	ENET_TX_D2	AA8	2.5-V CMOS	RGMII transmit data bus
16	ENET_TX_D3	AG8	2.5-V CMOS	RGMII transmit data bus
9	ENET_TX_EN	K20	2.5-V CMOS	RGMII transmit enable
55	ENET_XTAL_25MHZ	—	2.5-V CMOS	25-MHz RGMII transmit clock
29	MDI_P0	—	2.5-V CMOS	Media dependent interface
31	MDI_N0	—	2.5-V CMOS	Media dependent interface
33	MDI_P1	—	2.5-V CMOS	Media dependent interface
34	MDI_N1	—	2.5-V CMOS	Media dependent interface
39	MDI_P2	—	2.5-V CMOS	Media dependent interface
41	MDI_N2	—	2.5-V CMOS	Media dependent interface
42	MDI_P3	—	2.5-V CMOS	Media dependent interface
43	MDI_N3	—	2.5-V CMOS	Media dependent interface

HSMC

The development board supports a HSMC interface. This physical interface provides four channels of 3.125 Gbps-capable transceivers. The HSMC interface also supports a full SPI4.2 interface (17 LVDS channels), three input and output clocks, as well as JTAG and SMB signals. The LVDS channels can be used for CMOS signaling or LVDS.

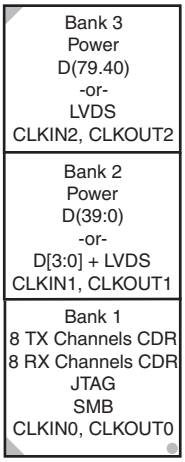
The HSMC is an Altera-developed open specification, which allows you to expand the functionality of the development board through the addition of daughtercards (HSMCs).

For more information about the HSMC specification such as signaling standards, signal integrity, compatible connectors, and mechanical information, refer to the *High Speed Mezzanine Card (HSMC) Specification* manual.

The HSMC connector has a total of 172 pins, including 120 signal pins, 39 power pins, and 13 ground pins. The ground pins are located between the two rows of signal and power pins, acting both as a shield and a reference. The HSMC host connector is based on the 0.5 mm-pitch QSH/QTH family of high-speed, board-to-board connectors from Samtec. There are three banks in this connector. Bank 1 has every third pin removed as done in the QSH-DP/QTH-DP series. Bank 2 and bank 3 have all the pins populated as done in the QSH/QTH series.

Figure 2–8 shows the bank arrangement of signals with respect to the Samtec connector's three banks.

Figure 2–8. HSMC Signal and Bank Diagram



The HSMC interface has programmable bi-directional I/O pins that can be used as 2.5-V LVCMOS, which is 3.3-V LVTTL-compatible. These pins can also be used as various differential I/O standards including, but not limited to, LVDS, mini-LVDS, and RSDS with up to 17 full-duplex channels.

☞ As noted in the *High Speed Mezzanine Card (HSMC) Specification* manual, LVDS and single-ended I/O standards are only guaranteed to function when mixed according to either the generic single-ended pin-out or generic differential pin-out.

Table 2–24 lists the HSMC interface pin assignments, signal names, and functions.

Table 2–24. HSMC Interface Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 4)

Board Reference (J1)	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
17	HSMA_TX_P3	K4	1.5-V PCML	Transceiver TX bit 3
18	HSMA_RX_P3	L2	1.5-V PCML	Transceiver RX bit 3
19	HSMA_TX_N3	K3	1.5-V PCML	Transceiver TX bit 3n
20	HSMA_RX_N3	L1	1.5-V PCML	Transceiver RX bit 3n
21	HSMA_TX_P2	M4	1.5-V PCML	Transceiver TX bit 2
22	HSMA_RX_P2	N2	1.5-V PCML	Transceiver RX bit 2
23	HSMA_TX_N2	M3	1.5-V PCML	Transceiver TX bit 2n
24	HSMA_RX_N2	N1	1.5-V PCML	Transceiver RX bit 2n

Table 2–24. HSMC Interface Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 4)

Board Reference (J1)	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
25	HSMA_TX_P1	P4	1.5-V PCML	Transceiver TX bit 1
26	HSMA_RX_P1	R2	1.5-V PCML	Transceiver RX bit 1
27	HSMA_TX_N1	P3	1.5-V PCML	Transceiver TX bit 1n
28	HSMA_RX_N1	R1	1.5-V PCML	Transceiver RX bit 1n
29	HSMA_TX_P0	T4	1.5-V PCML	Transceiver TX bit 0
30	HSMA_RX_P0	U2	1.5-V PCML	Transceiver RX bit 0
31	HSMA_TX_N0	T3	1.5-V PCML	Transceiver TX bit 0n
32	HSMA_RX_N0	U1	1.5-V PCML	Transceiver RX bit 0n
33	HSMA_SDA	H14	2.5-V CMOS	Management serial data
34	HSMA_SCL	J14	2.5-V CMOS	Management serial clock
35	JTAG_TCK	AC7	2.5-V CMOS	JTAG clock signal
36	HSMA_JTAG_TMS	—	2.5-V CMOS	JTAG mode select signal
37	HSMA_JTAG_TDO	—	2.5-V CMOS	JTAG data output
38	JTAG_FPGA_TDO_RETIMER	—	2.5-V CMOS	JTAG data input
39	HSMA_CLK_OUT0	J19	2.5-V CMOS	Dedicated CMOS clock out
40	HSMA_CLK_IN0	L15	2.5-V CMOS	Dedicated CMOS clock in
41	HSMA_D0	K16	2.5-V CMOS	Dedicated CMOS I/O bit 0
42	HSMA_D1	L18	2.5-V CMOS	Dedicated CMOS I/O bit 1
43	HSMA_D2	K18	2.5-V CMOS	Dedicated CMOS I/O bit 2
44	HSMA_D3	K17	2.5-V CMOS	Dedicated CMOS I/O bit 3
47	HSMA_TX_D_P0	D12	LVDS or 2.5-V	LVDS TX bit 0 or CMOS bit 4
48	HSMA_RX_D_P0	E11	LVDS or 2.5-V	LVDS RX bit 0 or CMOS bit 5
49	HSMA_TX_D_N0	C12	LVDS or 2.5-V	LVDS TX bit 0n or CMOS bit 6
50	HSMA_RX_D_N0	D10	LVDS or 2.5-V	LVDS RX bit 0n or CMOS bit 7
53	HSMA_TX_D_P1	D14	LVDS or 2.5-V	LVDS TX bit 1 or CMOS bit 8
54	HSMA_RX_D_P1	H12	LVDS or 2.5-V	LVDS RX bit 1 or CMOS bit 9
55	HSMA_TX_D_N1	C14	LVDS or 2.5-V	LVDS TX bit 1n or CMOS bit 10
56	HSMA_RX_D_N1	G12	LVDS or 2.5-V	LVDS RX bit 1n or CMOS bit 11
59	HSMA_TX_D_P2	B13	LVDS or 2.5-V	LVDS TX bit 2 or CMOS bit 12
60	HSMA_RX_D_P2	E12	LVDS or 2.5-V	LVDS RX bit 2 or CMOS bit 13
61	HSMA_TX_D_N2	A13	LVDS or 2.5-V	LVDS TX bit 2n or CMOS bit 14
62	HSMA_RX_D_N2	D13	LVDS or 2.5-V	LVDS RX bit 2n or CMOS bit 15
65	HSMA_TX_D_P3	B14	LVDS or 2.5-V	LVDS TX bit 3 or CMOS bit 16
66	HSMA_RX_D_P3	G14	LVDS or 2.5-V	LVDS RX bit 3 or CMOS bit 17
67	HSMA_TX_D_N3	A14	LVDS or 2.5-V	LVDS TX bit 3n or CMOS bit 18
68	HSMA_RX_D_N3	F14	LVDS or 2.5-V	LVDS RX bit 3n or CMOS bit 19
71	HSMA_TX_D_P4	A16	LVDS or 2.5-V	LVDS TX bit 4 or CMOS bit 20
72	HSMA_RX_D_P4	F15	LVDS or 2.5-V	LVDS RX bit 4 or CMOS bit 21
73	HSMA_TX_D_N4	A15	LVDS or 2.5-V	LVDS TX bit 4n or CMOS bit 22

Table 2–24. HSMC Interface Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 4)

Board Reference (J1)	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
74	HSMA_RX_D_N4	E15	LVDS or 2.5-V	LVDS RX bit 4n or CMOS bit 23
77	HSMA_TX_D_P5	E23	LVDS or 2.5-V	LVDS TX bit 5 or CMOS bit 24
78	HSMA_RX_D_P5	C16	LVDS or 2.5-V	LVDS RX bit 5 or CMOS bit 25
79	HSMA_TX_D_N5	D22	LVDS or 2.5-V	LVDS TX bit 5n or CMOS bit 26
80	HSMA_RX_D_N5	C15	LVDS or 2.5-V	LVDS RX bit 5n or CMOS bit 27
83	HSMA_TX_D_P6	B18	LVDS or 2.5-V	LVDS TX bit 6 or CMOS bit 28
84	HSMA_RX_D_P6	F16	LVDS or 2.5-V	LVDS RX bit 6 or CMOS bit 29
85	HSMA_TX_D_N6	A18	LVDS or 2.5-V	LVDS TX bit 6n or CMOS bit 30
86	HSMA_RX_D_N6	E16	LVDS or 2.5-V	LVDS RX bit 6n or CMOS bit 31
89	HSMA_TX_D_P7	B19	LVDS or 2.5-V	LVDS TX bit 7 or CMOS bit 32
90	HSMA_RX_D_P7	G18	LVDS or 2.5-V	LVDS RX bit 7 or CMOS bit 33
91	HSMA_TX_D_N7	A19	LVDS or 2.5-V	LVDS TX bit 7n or CMOS bit 34
92	HSMA_RX_D_N7	F18	LVDS or 2.5-V	LVDS RX bit 7n or CMOS bit 35
95	HSMA_CLK_OUT_P1	B26	LVDS or 2.5-V	LVDS or CMOS clock out 1 or CMOS bit 36
96	HSMA_CLK_IN_P1	H19	LVDS or 2.5-V	LVDS or CMOS clock in 1 or CMOS bit 37
97	HSMA_CLK_OUT_N1	A26	LVDS or 2.5-V	LVDS or CMOS clock out 1 or CMOS bit 38
98	HSMA_CLK_IN_N1	J18	LVDS or 2.5-V	LVDS or CMOS clock in 1 or CMOS bit 39
101	HSMA_TX_D_P8	B22	LVDS or 2.5-V	LVDS TX bit 8 or CMOS bit 40
102	HSMA_RX_D_P8	F19	LVDS or 2.5-V	LVDS RX bit 8 or CMOS bit 41
103	HSMA_TX_D_N8	B21	LVDS or 2.5-V	LVDS TX bit 8n or CMOS bit 42
104	HSMA_RX_D_N8	E18	LVDS or 2.5-V	LVDS RX bit 8n or CMOS bit 43
107	HSMA_TX_D_P9	A21	LVDS or 2.5-V	LVDS TX bit 9 or CMOS bit 44
108	HSMA_RX_D_P9	D20	LVDS or 2.5-V	LVDS RX bit 9 or CMOS bit 45
109	HSMA_TX_D_N9	A20	LVDS or 2.5-V	LVDS TX bit 9n or CMOS bit 46
110	HSMA_RX_D_N9	C19	LVDS or 2.5-V	LVDS RX bit 9n or CMOS bit 47
113	HSMA_TX_D_P10	D23	LVDS or 2.5-V	LVDS TX bit 10 or CMOS bit 48
114	HSMA_RX_D_P10	C21	LVDS or 2.5-V	LVDS RX bit 10 or CMOS bit 49
115	HSMA_TX_D_N10	C22	LVDS or 2.5-V	LVDS TX bit 10n or CMOS bit 50
116	HSMA_RX_D_N10	C20	LVDS or 2.5-V	LVDS RX bit 10n or CMOS bit 51
119	HSMA_TX_D_P11	B23	LVDS or 2.5-V	LVDS TX bit 11 or CMOS bit 52
120	HSMA_RX_D_P11	F20	LVDS or 2.5-V	LVDS RX bit 11 or CMOS bit 53
121	HSMA_TX_D_N11	A23	LVDS or 2.5-V	LVDS TX bit 11n or CMOS bit 54
122	HSMA_RX_D_N11	E20	LVDS or 2.5-V	LVDS RX bit 11n or CMOS bit 55
125	HSMA_TX_D_P12	C24	LVDS or 2.5-V	LVDS TX bit 12 or CMOS bit 56
126	HSMA_RX_D_P12	E22	LVDS or 2.5-V	LVDS RX bit 12 or CMOS bit 57
127	HSMA_TX_D_N12	B24	LVDS or 2.5-V	LVDS TX bit 12n or CMOS bit 58
128	HSMA_RX_D_N12	E21	LVDS or 2.5-V	LVDS RX bit 12n or CMOS bit 59
131	HSMA_TX_D_P13	D25	LVDS or 2.5-V	LVDS TX bit 13 or CMOS bit 60
132	HSMA_RX_D_P13	L20	LVDS or 2.5-V	LVDS RX bit 13 or CMOS bit 61

Table 2–24. HSMC Interface Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 4)

Board Reference (J1)	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
133	HSMA_TX_D_N13	C25	LVDS or 2.5-V	LVDS TX bit 13n or CMOS bit 62
134	HSMA_RX_D_N13	L19	LVDS or 2.5-V	LVDS RX bit 13n or CMOS bit 63
137	HSMA_TX_D_P14	C27	LVDS or 2.5-V	LVDS TX bit 14 or CMOS bit 64
138	HSMA_RX_D_P14	G22	LVDS or 2.5-V	LVDS RX bit 14 or CMOS bit 65
139	HSMA_TX_D_N14	C26	LVDS or 2.5-V	LVDS TX bit 14n or CMOS bit 66
140	HSMA_RX_D_N14	G23	LVDS or 2.5-V	LVDS RX bit 14n or CMOS bit 67
143	HSMA_TX_D_P15	B27	LVDS or 2.5-V	LVDS TX bit 15 or CMOS bit 68
144	HSMA_RX_D_P15	H21	LVDS or 2.5-V	LVDS RX bit 15 or CMOS bit 69
145	HSMA_TX_D_N15	A28	LVDS or 2.5-V	LVDS TX bit 15n or CMOS bit 70
146	HSMA_RX_D_N15	G21	LVDS or 2.5-V	LVDS RX bit 15n or CMOS bit 71
149	HSMA_TX_D_P16	E26	LVDS or 2.5-V	LVDS TX bit 16 or CMOS bit 72
150	HSMA_RX_D_P16	J20	LVDS or 2.5-V	LVDS RX bit 16 or CMOS bit 73
151	HSMA_TX_D_N16	E25	LVDS or 2.5-V	LVDS TX bit 16n or CMOS bit 74
152	HSMA_RX_D_N16	H20	LVDS or 2.5-V	LVDS RX bit 16n or CMOS bit 75
155	HSMA_CLK_OUT_P2	A25	LVDS or 2.5-V	LVDS or CMOS clock out 2 or CMOS bit 76
156	HSMA_CLK_IN_P2	L14	LVDS or 2.5-V	LVDS or CMOS clock in 2 or CMOS bit 77
157	HSMA_CLK_OUT_N2	A24	LVDS or 2.5-V	LVDS or CMOS clock out 2 or CMOS bit 78
158	HSMA_CLK_IN_N2	L13	LVDS or 2.5-V	LVDS or CMOS clock in 2 or CMOS bit 79
160	HSMA_PRSNTn	L16	2.5-V CMOS	HSMC port A presence detect

SDI Video Output/Input

The SDI video port consists of a LMH0303 cable driver and a LMH0384 cable equalizer. The PHY devices from National Semiconductor interface to single-ended 75-Ω SMB connectors.

The cable driver supports operation at 270 Mbit standard definition (SD), 1.5 Gbit high definition (HD), and 2.97 Gbit dual-link HD modes. Control signals are allowed for SD and HD modes selections, as well as device enable. The reference clock of the device is 148.5 MHz and matches the incoming signals to within 50 ppm using the UP and DN voltage control lines to the voltage-controlled crystal oscillator (VCXO).

Table 2–25 lists the supported output standards for the SD and HD input.

Table 2–25. Supported Output Standards for SD and HD Input

SD_HD Input	Supported Output Standards	Rise TIme
0	SMPTE 424M, SMPTE 292M	Faster
1	SMPTE 259M	Slower

For more information about the application circuit of the cable driver, refer to the cable driver data sheet in www.national.com.

Table 2–26 summarizes the SDI video output interface pin assignments, signal names, and functions.

Table 2–26. SDI Video Output Interface Pin Assignments, Schematic Signal Names, and Functions

Board Reference (U1)	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
1	SDI_TX_P	V4	1.5-V PCML	Serial data input P
2	SDI_TX_N	V3	1.5-V PCML	Serial data input N
4	SDI_TX_RSET	—	2.5-V	Output swing set resistor
6	SDI_TX_EN	AJ1	2.5-V	Output driver enable
7	SDI_SDA	R20	2.5-V	Cable driver I²C bus
8	SDI_SCL	T21	2.5-V	Cable driver I²C bus
10	SDI_TX_SD_HDN	AF7	2.5-V	High-definition select
11	SDI_TXDRV_N	—	2.5-V	Serial data
12	SDI_TXDRV_P	—	2.5-V	Serial data
13	SDI_FAULT	F25	2.5-V	Data transmission fault

The cable equalizer supports operation at 270 Mbit SD, 1.5 Gbit HD, and 2.97 Gbit dual-link HD modes. Control signals are allowed for bypassing or disabling the device, as well as a carrier detect or auto-mute signal interface.

Table 2–27 lists the cable equalizer lengths.

Table 2–27. SDI Cable Equalizer Lengths

Data Rate (Mbps)	Cable Type	Maximum Cable Length (m)
270	Belden 1694A	400
1485		140
2970		120

Figure 2–9 shows the SDI cable equalizer, which is an excerpt from the LMH0384 cable equalizer data sheet. On this development board, the output is a single-ended output, with the negative channel driving a load local to the board.

Figure 2–9. SDI Cable Equalizer

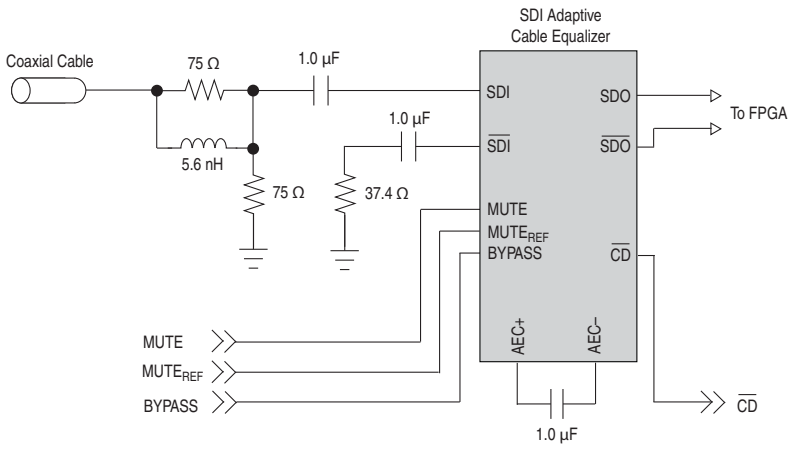


Table 2–28 summarizes the SDI video input interface pin assignments, signal names, and functions.

Table 2–28. SDI Video Input Interface Pin Assignments, Schematic Signal Names, and Functions

Board Reference (U4)	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
7	SDI_RX_BYPASS	AF10	2.5-V	Equalizer bypass enable
10	SDI_RX_N	W1	1.5-V PCML	Serial data output N
11	SDI_RX_P	W2	1.5-V PCML	Serial data output P
14	SDI_RX_EN	AE10	2.5-V	Device enable

Memory

This section describes the development board's memory interface support and also their signal names, types, and connectivity relative to the Cyclone V GX. The development board has the following memory interfaces:

- DDR3 SDRAM
- Synchronous SRAM
- Synchronous flash

For more information about the memory interfaces, refer to the following documents:

- *Timing Analysis* section in the External Memory Interface Handbook.
- *DDR, DDR2, and DDR3 SDRAM Design Tutorials* section in the External Memory Interface Handbook.

DDR3 SDRAM

The development board supports four 16Mx16x8 and two16Mx8x8 DDR3 SDRAM interfaces for very high-speed sequential memory access. The DDR3 SDRAM has two independent interfaces:

- DDR3A x32 interface using a hard memory controller (vertical I/O banks on the bottom edge of the FPGA).
- DDR3B x32 interface using a soft memory controller (horizontal I/O banks on the right edge of the FPGA).

Each 32-bit data bus comprises of two x16 devices and one x8 device for ECC support.

With a soft memory controller, this memory interface runs at a target frequency of 333 MHz for a maximum theoretical bandwidth of over 21.31 Gbps. The maximum frequency for this DDR3 device is 667 MHz with a CAS latency of 9.

Table 2–29 lists the DDR3A pin assignments, signal names, and functions. The signal names and types are relative to the Cyclone V GX in terms of I/O setting and direction.

Table 2–29. DDR3A Device Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 4)

Board Reference	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
DDR3 x16 (U21)				
N3	DDR3A_A0	AJ12	1.5-V SSTL Class I	Address bus
P7	DDR3A_A1	AK12	1.5-V SSTL Class I	Address bus
P3	DDR3A_A2	AH11	1.5-V SSTL Class I	Address bus
N2	DDR3A_A3	AH12	1.5-V SSTL Class I	Address bus
P8	DDR3A_A4	AG13	1.5-V SSTL Class I	Address bus
P2	DDR3A_A5	AG14	1.5-V SSTL Class I	Address bus
R8	DDR3A_A6	AK10	1.5-V SSTL Class I	Address bus
R2	DDR3A_A7	AK11	1.5-V SSTL Class I	Address bus
T8	DDR3A_A8	AF11	1.5-V SSTL Class I	Address bus
R3	DDR3A_A9	AG11	1.5-V SSTL Class I	Address bus
L7	DDR3A_A10	AJ8	1.5-V SSTL Class I	Address bus
R7	DDR3A_A11	AK8	1.5-V SSTL Class I	Address bus
N7	DDR3A_A12	AJ7	1.5-V SSTL Class I	Address bus
T3	DDR3A_A13	AK7	1.5-V SSTL Class I	Address bus
M2	DDR3A_BA0	AH9	1.5-V SSTL Class I	Bank address bus
N8	DDR3A_BA1	AH10	1.5-V SSTL Class I	Bank address bus
M3	DDR3A_BA2	AJ10	1.5-V SSTL Class I	Bank address bus
K3	DDR3A_CASN	AF9	1.5-V SSTL Class I	Row address select
K9	DDR3A_CKE	AK18	1.5-V SSTL Class I	Column address select
J7	DDR3A_CLK_P	Y13	Differential 1.5-V SSTL Class I	Differential output clock
K7	DDR3A_CLK_N	AA14	Differential 1.5-V SSTL Class I	Differential output clock
L2	DDR3A_CSN	Y12	1.5-V SSTL Class I	Chip select
E7	DDR3A_DM0	AE15	1.5-V SSTL Class I	Write mask byte lane
D3	DDR3A_DM1	AH19	1.5-V SSTL Class I	Write mask byte lane
E3	DDR3A_DQ0	AF15	1.5-V SSTL Class I	Data bus byte lane 0
H8	DDR3A_DQ1	AE16	1.5-V SSTL Class I	Data bus byte lane 0
F7	DDR3A_DQ2	AJ14	1.5-V SSTL Class I	Data bus byte lane 0
H7	DDR3A_DQ3	AH15	1.5-V SSTL Class I	Data bus byte lane 0
F2	DDR3A_DQ4	AE17	1.5-V SSTL Class I	Data bus byte lane 0
G2	DDR3A_DQ5	AD17	1.5-V SSTL Class I	Data bus byte lane 0
F8	DDR3A_DQ6	AJ15	1.5-V SSTL Class I	Data bus byte lane 0
H3	DDR3A_DQ7	AF14	1.5-V SSTL Class I	Data bus byte lane 0
A7	DDR3A_DQ8	AK17	1.5-V SSTL Class I	Data bus byte lane 1

Table 2–29. DDR3A Device Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 4)

Board Reference	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
C3	DDR3A_DQ9	AK16	1.5-V SSTL Class I	Data bus byte lane 1
A3	DDR3A_DQ10	AG17	1.5-V SSTL Class I	Data bus byte lane 1
D7	DDR3A_DQ11	AJ18	1.5-V SSTL Class I	Data bus byte lane 1
A2	DDR3A_DQ12	AG16	1.5-V SSTL Class I	Data bus byte lane 1
C2	DDR3A_DQ13	AF16	1.5-V SSTL Class I	Data bus byte lane 1
B8	DDR3A_DQ14	AJ19	1.5-V SSTL Class I	Data bus byte lane 1
C8	DDR3A_DQ15	AH20	1.5-V SSTL Class I	Data bus byte lane 1
F3	DDR3A_DQS_P0	Y16	Differential 1.5-V SSTL Class I	Data strobe P byte lane 0
G3	DDR3A_DQS_N0	AA16	Differential 1.5-V SSTL Class I	Data strobe N byte lane 0
C7	DDR3A_DQS_P1	Y17	Differential 1.5-V SSTL Class I	Data strobe P byte lane 1
B7	DDR3A_DQS_N1	Y18	Differential 1.5-V SSTL Class I	Data strobe N byte lane 1
K1	DDR3A_ODT	AH14	1.5-V SSTL Class I	On-die termination enable
J3	DDR3A_RASN	AG9	1.5-V SSTL Class I	Row address select
T2	DDR3A_RESETN	AK21	1.5-V SSTL Class I	Reset
L3	DDR3A_WEN	AK5	1.5-V SSTL Class I	Write enable
L8	DDR3A_ZQ01	—	1.5-V SSTL Class I	ZQ impedance calibration
DDR3 x16 (U22)				
N3	DDR3A_A0	AJ12	1.5-V SSTL Class I	Address bus
P7	DDR3A_A1	AK12	1.5-V SSTL Class I	Address bus
P3	DDR3A_A2	AH11	1.5-V SSTL Class I	Address bus
N2	DDR3A_A3	AH12	1.5-V SSTL Class I	Address bus
P8	DDR3A_A4	AG13	1.5-V SSTL Class I	Address bus
P2	DDR3A_A5	AG14	1.5-V SSTL Class I	Address bus
R8	DDR3A_A6	AK10	1.5-V SSTL Class I	Address bus
R2	DDR3A_A7	AK11	1.5-V SSTL Class I	Address bus
T8	DDR3A_A8	AF11	1.5-V SSTL Class I	Address bus
R3	DDR3A_A9	AG11	1.5-V SSTL Class I	Address bus
L7	DDR3A_A10	AJ8	1.5-V SSTL Class I	Address bus
R7	DDR3A_A11	AK8	1.5-V SSTL Class I	Address bus
N7	DDR3A_A12	AJ7	1.5-V SSTL Class I	Address bus
T3	DDR3A_A13	AK7	1.5-V SSTL Class I	Address bus
M2	DDR3A_BA0	AH9	1.5-V SSTL Class I	Bank address bus
N8	DDR3A_BA1	AH10	1.5-V SSTL Class I	Bank address bus
M3	DDR3A_BA2	AJ10	1.5-V SSTL Class I	Bank address bus
K3	DDR3A_CASN	AF9	1.5-V SSTL Class I	Row address select

Table 2–29. DDR3A Device Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 4)

Board Reference	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
K9	DDR3A_CKE	AK18	1.5-V SSTL Class I	Column address select
K7	DDR3A_CLK_P	Y13	1.5-V SSTL Class I	Differential output clock
J7	DDR3A_CLK_N	AA14	1.5-V SSTL Class I	Differential output clock
L2	DDR3A_CSN	Y12	1.5-V SSTL Class I	Chip select
E7	DDR3A_DM2	AJ23	1.5-V SSTL Class I	Write mask byte lane
D3	DDR3A_DM3	AJ27	1.5-V SSTL Class I	Write mask byte lane
F2	DDR3A_DQ16	AE18	1.5-V SSTL Class I	Data bus byte lane 2
F8	DDR3A_DQ17	AD18	1.5-V SSTL Class I	Data bus byte lane 2
E3	DDR3A_DQ18	AJ20	1.5-V SSTL Class I	Data bus byte lane 2
F7	DDR3A_DQ19	AK22	1.5-V SSTL Class I	Data bus byte lane 2
H3	DDR3A_DQ20	AF19	1.5-V SSTL Class I	Data bus byte lane 2
G2	DDR3A_DQ21	AF18	1.5-V SSTL Class I	Data bus byte lane 2
H7	DDR3A_DQ22	AH21	1.5-V SSTL Class I	Data bus byte lane 2
H8	DDR3A_DQ23	AK23	1.5-V SSTL Class I	Data bus byte lane 2
A2	DDR3A_DQ24	AG19	1.5-V SSTL Class I	Data bus byte lane 3
C2	DDR3A_DQ25	AG18	1.5-V SSTL Class I	Data bus byte lane 3
D7	DDR3A_DQ26	AH24	1.5-V SSTL Class I	Data bus byte lane 3
A7	DDR3A_DQ27	AK25	1.5-V SSTL Class I	Data bus byte lane 3
A3	DDR3A_DQ28	AE20	1.5-V SSTL Class I	Data bus byte lane 3
C3	DDR3A_DQ29	AD19	1.5-V SSTL Class I	Data bus byte lane 3
B8	DDR3A_DQ30	AG24	1.5-V SSTL Class I	Data bus byte lane 3
C8	DDR3A_DQ31	AK26	1.5-V SSTL Class I	Data bus byte lane 3
F3	DDR3A_DQS_P2	Y20	Differential 1.5-V SSTL Class I	Data strobe P byte lane 2
G3	DDR3A_DQS_N2	AA20	Differential 1.5-V SSTL Class I	Data strobe N byte lane 2
C7	DDR3A_DQS_P3	AB19	Differential 1.5-V SSTL Class I	Data strobe P byte lane 3
B7	DDR3A_DQS_N3	AC19	Differential 1.5-V SSTL Class I	Data strobe N byte lane 3
K1	DDR3A_ODT	AH14	1.5-V SSTL Class I	On-die termination enable
J3	DDR3A_RASN	AG9	1.5-V SSTL Class I	Row address select
T2	DDR3A_RESETN	AK21	1.5-V SSTL Class I	Reset
L3	DDR3A_WEN	AK5	1.5-V SSTL Class I	Write enable
L8	DDR3A_ZQ2	—	1.5-V SSTL Class I	ZQ impedance calibration
DDR3 x8 (U23)				
K3	DDR3A_A0	AJ12	1.5-V SSTL Class I	Address bus
L7	DDR3A_A1	AK12	1.5-V SSTL Class I	Address bus
L3	DDR3A_A2	AH11	1.5-V SSTL Class I	Address bus

Table 2–29. DDR3A Device Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 4)

Board Reference	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
K2	DDR3A_A3	AH12	1.5-V SSTL Class I	Address bus
L8	DDR3A_A4	AG13	1.5-V SSTL Class I	Address bus
L2	DDR3A_A5	AG14	1.5-V SSTL Class I	Address bus
M8	DDR3A_A6	AK10	1.5-V SSTL Class I	Address bus
M2	DDR3A_A7	AK11	1.5-V SSTL Class I	Address bus
N8	DDR3A_A8	AF11	1.5-V SSTL Class I	Address bus
M3	DDR3A_A9	AG11	1.5-V SSTL Class I	Address bus
H7	DDR3A_A10	AJ8	1.5-V SSTL Class I	Address bus
M7	DDR3A_A11	AK8	1.5-V SSTL Class I	Address bus
K7	DDR3A_A12	AJ7	1.5-V SSTL Class I	Address bus
N3	DDR3A_A13	AK7	1.5-V SSTL Class I	Address bus
J2	DDR3A_BA0	AH9	1.5-V SSTL Class I	Bank address bus
K8	DDR3A_BA1	AH10	1.5-V SSTL Class I	Bank address bus
J3	DDR3A_BA2	AJ10	1.5-V SSTL Class I	Bank address bus
G3	DDR3A_CASN	AF9	1.5-V SSTL Class I	Row address select
G9	DDR3A_CKE	AK18	1.5-V SSTL Class I	Column address select
G7	DDR3A_CLK_N	Y13	1.5-V SSTL Class I	Differential output clock
F7	DDR3A_CLK_P	AA14	1.5-V SSTL Class I	Differential output clock
H2	DDR3A_CSN	Y12	1.5-V SSTL Class I	Chip select
B7	DDR3A_DM4	AG23	1.5-V SSTL Class I	Write mask byte lane
E3	DDR3A_DQ32	AG21	1.5-V SSTL Class I	Data bus byte lane 4
C8	DDR3A_DQ33	AF20	1.5-V SSTL Class I	Data bus byte lane 4
E7	DDR3A_DQ34	AK27	1.5-V SSTL Class I	Data bus byte lane 4
B3	DDR3A_DQ35	AH26	1.5-V SSTL Class I	Data bus byte lane 4
D2	DDR3A_DQ36	AG22	1.5-V SSTL Class I	Data bus byte lane 4
C7	DDR3A_DQ37	AF21	1.5-V SSTL Class I	Data bus byte lane 4
E8	DDR3A_DQ38	AE22	1.5-V SSTL Class I	Data bus byte lane 4
C2	DDR3A_DQ39	AH22	1.5-V SSTL Class I	Data bus byte lane 4
D3	DDR3A_DQS_N4	AD20	Differential 1.5-V SSTL Class I	Data strobe P byte lane 4
C3	DDR3A_DQS_P4	AC21	Differential 1.5-V SSTL Class I	Data strobe N byte lane 4
G1	DDR3A_ODT	AH14	1.5-V SSTL Class I	On-die termination enable
F3	DDR3A_RASN	AG9	1.5-V SSTL Class I	Row address select
N2	DDR3A_RESETN	AK21	1.5-V SSTL Class I	Reset
H3	DDR3A_WEN	AK5	1.5-V SSTL Class I	Write enable
H8	DDR3A_ZQ05	—	1.5-V SSTL Class I	ZQ impedance calibration

Table 2–29 lists the DDR3B pin assignments, signal names, and functions. The signal names and types are relative to the Cyclone V GX in terms of I/O setting and direction.

Table 2–30. DDR3B Device Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 4)

Board Reference	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
DDR3 x16 (U6)				
N3	DDR3B_A0	Y30	1.5-V SSTL Class I	Address bus
P7	DDR3B_A1	R28	1.5-V SSTL Class I	Address bus
P3	DDR3B_A2	AA29	1.5-V SSTL Class I	Address bus
N2	DDR3B_A3	W29	1.5-V SSTL Class I	Address bus
P8	DDR3B_A4	U23	1.5-V SSTL Class I	Address bus
P2	DDR3B_A5	AA30	1.5-V SSTL Class I	Address bus
R8	DDR3B_A6	R23	1.5-V SSTL Class I	Address bus
R2	DDR3B_A7	AC30	1.5-V SSTL Class I	Address bus
T8	DDR3B_A8	T23	1.5-V SSTL Class I	Address bus
R3	DDR3B_A9	AB29	1.5-V SSTL Class I	Address bus
L7	DDR3B_A10	R30	1.5-V SSTL Class I	Address bus
R7	DDR3B_A11	R26	1.5-V SSTL Class I	Address bus
N7	DDR3B_A12	T25	1.5-V SSTL Class I	Address bus
T3	DDR3B_A13	AD29	1.5-V SSTL Class I	Address bus
M2	DDR3B_BA0	W30	1.5-V SSTL Class I	Bank address bus
N8	DDR3B_BA1	T24	1.5-V SSTL Class I	Bank address bus
M3	DDR3B_BA2	V30	1.5-V SSTL Class I	Bank address bus
K3	DDR3B_CASN	T30	1.5-V SSTL Class I	Row address select
K9	DDR3B_CKE	L28	1.5-V SSTL Class I	Column address select
J7	DDR3B_CLK_P	P22	Differential 1.5-V SSTL Class I	Differential output clock
K7	DDR3B_CLK_N	P23	Differential 1.5-V SSTL Class I	Differential output clock
L2	DDR3B_CSN	U29	1.5-V SSTL Class I	Chip select
E7	DDR3B_DM0	C29	1.5-V SSTL Class I	Write mask byte lane
D3	DDR3B_DM1	D29	1.5-V SSTL Class I	Write mask byte lane
E3	DDR3B_DQ0	D30	1.5-V SSTL Class I	Data bus byte lane 0
F7	DDR3B_DQ1	C30	1.5-V SSTL Class I	Data bus byte lane 0
F2	DDR3B_DQ2	F29	1.5-V SSTL Class I	Data bus byte lane 0
F8	DDR3B_DQ3	K22	1.5-V SSTL Class I	Data bus byte lane 0
H3	DDR3B_DQ4	E28	1.5-V SSTL Class I	Data bus byte lane 0
H8	DDR3B_DQ5	K21	1.5-V SSTL Class I	Data bus byte lane 0
G2	DDR3B_DQ6	G29	1.5-V SSTL Class I	Data bus byte lane 0
H7	DDR3B_DQ7	L23	1.5-V SSTL Class I	Data bus byte lane 0
D7	DDR3B_DQ8	J23	1.5-V SSTL Class I	Data bus byte lane 1

Table 2–30. DDR3B Device Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 4)

Board Reference	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
C3	DDR3B_DQ9	D28	1.5-V SSTL Class I	Data bus byte lane 1
C8	DDR3B_DQ10	A29	1.5-V SSTL Class I	Data bus byte lane 1
C2	DDR3B_DQ11	H25	1.5-V SSTL Class I	Data bus byte lane 1
A7	DDR3B_DQ12	H24	1.5-V SSTL Class I	Data bus byte lane 1
A2	DDR3B_DQ13	H26	1.5-V SSTL Class I	Data bus byte lane 1
B8	DDR3B_DQ14	B28	1.5-V SSTL Class I	Data bus byte lane 1
A3	DDR3B_DQ15	D27	1.5-V SSTL Class I	Data bus byte lane 1
F3	DDR3B_DQS_P0	N21	Differential 1.5-V SSTL Class I	Data strobe P byte lane 0
G3	DDR3B_DQS_N0	M22	Differential 1.5-V SSTL Class I	Data strobe N byte lane 0
C7	DDR3B_DQS_P1	P20	Differential 1.5-V SSTL Class I	Data strobe P byte lane 1
B7	DDR3B_DQS_N1	N20	Differential 1.5-V SSTL Class I	Data strobe N byte lane 1
K1	DDR3B_ODT	V29	1.5-V SSTL Class I	On-die termination enable
J3	DDR3B_RASN	T29	1.5-V SSTL Class I	Row address select
T2	DDR3B_RESETN	AB27	1.5-V SSTL Class I	Reset
L3	DDR3B_WEN	T28	1.5-V SSTL Class I	Write enable
L8	DDR3B_ZQ01	—	1.5-V SSTL Class I	ZQ impedance calibration
DDR3 x16 (U15)				
N3	DDR3B_A0	Y30	1.5-V SSTL Class I	Address bus
P7	DDR3B_A1	R28	1.5-V SSTL Class I	Address bus
P3	DDR3B_A2	AA29	1.5-V SSTL Class I	Address bus
N2	DDR3B_A3	W29	1.5-V SSTL Class I	Address bus
P8	DDR3B_A4	U23	1.5-V SSTL Class I	Address bus
P2	DDR3B_A5	AA30	1.5-V SSTL Class I	Address bus
R8	DDR3B_A6	R23	1.5-V SSTL Class I	Address bus
R2	DDR3B_A7	AC30	1.5-V SSTL Class I	Address bus
T8	DDR3B_A8	T23	1.5-V SSTL Class I	Address bus
R3	DDR3B_A9	AB29	1.5-V SSTL Class I	Address bus
L7	DDR3B_A10	R30	1.5-V SSTL Class I	Address bus
R7	DDR3B_A11	R26	1.5-V SSTL Class I	Address bus
N7	DDR3B_A12	T25	1.5-V SSTL Class I	Address bus
T3	DDR3B_A13	AD29	1.5-V SSTL Class I	Address bus
M2	DDR3B_BA0	W30	1.5-V SSTL Class I	Bank address bus
N8	DDR3B_BA1	T24	1.5-V SSTL Class I	Bank address bus
M3	DDR3B_BA2	V30	1.5-V SSTL Class I	Bank address bus
K3	DDR3B_CASN	T30	1.5-V SSTL Class I	Row address select

Table 2–30. DDR3B Device Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 4)

Board Reference	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
K9	DDR3B_CKE	L28	1.5-V SSTL Class I	Column address select
K7	DDR3B_CLK_P	P22	1.5-V SSTL Class I	Differential output clock
J7	DDR3B_CLK_N	P23	1.5-V SSTL Class I	Differential output clock
L2	DDR3B_CSN	U29	1.5-V SSTL Class I	Chip select
E7	DDR3B_DM2	H30	1.5-V SSTL Class I	Write mask byte lane
D3	DDR3B_DM3	L30	1.5-V SSTL Class I	Write mask byte lane
E3	DDR3B_DQ16	J29	1.5-V SSTL Class I	Data bus byte lane 2
F7	DDR3B_DQ17	G26	1.5-V SSTL Class I	Data bus byte lane 2
F2	DDR3B_DQ18	J27	1.5-V SSTL Class I	Data bus byte lane 2
F8	DDR3B_DQ19	H29	1.5-V SSTL Class I	Data bus byte lane 2
H3	DDR3B_DQ20	J28	1.5-V SSTL Class I	Data bus byte lane 2
H8	DDR3B_DQ21	F30	1.5-V SSTL Class I	Data bus byte lane 2
G2	DDR3B_DQ22	K27	1.5-V SSTL Class I	Data bus byte lane 2
H7	DDR3B_DQ23	F26	1.5-V SSTL Class I	Data bus byte lane 2
D7	DDR3B_DQ24	J30	1.5-V SSTL Class I	Data bus byte lane 3
C3	DDR3B_DQ25	K25	1.5-V SSTL Class I	Data bus byte lane 3
C8	DDR3B_DQ26	G27	1.5-V SSTL Class I	Data bus byte lane 3
C2	DDR3B_DQ27	L25	1.5-V SSTL Class I	Data bus byte lane 3
A7	DDR3B_DQ28	L29	1.5-V SSTL Class I	Data bus byte lane 3
A2	DDR3B_DQ29	N27	1.5-V SSTL Class I	Data bus byte lane 3
B8	DDR3B_DQ30	K26	1.5-V SSTL Class I	Data bus byte lane 3
A3	DDR3B_DQ31	L26	1.5-V SSTL Class I	Data bus byte lane 3
F3	DDR3B_DQS_P2	N22	Differential 1.5-V SSTL Class I	Data strobe P byte lane 2
G3	DDR3B_DQS_N2	M23	Differential 1.5-V SSTL Class I	Data strobe N byte lane 2
C7	DDR3B_DQS_P3	N24	Differential 1.5-V SSTL Class I	Data strobe P byte lane 3
B7	DDR3B_DQS_N3	N25	Differential 1.5-V SSTL Class I	Data strobe N byte lane 3
K1	DDR3B_ODT	V29	1.5-V SSTL Class I	On-die termination enable
J3	DDR3B_RASN	T29	1.5-V SSTL Class I	Row address select
T2	DDR3B_RESETN	AB27	1.5-V SSTL Class I	Reset
L3	DDR3B_WEN	T28	1.5-V SSTL Class I	Write enable
L8	DDR3B_ZQ2	—	1.5-V SSTL Class I	ZQ impedance calibration
DDR3 x8 (U19)				
K3	DDR3B_A0	Y30	1.5-V SSTL Class I	Address bus
L7	DDR3B_A1	R28	1.5-V SSTL Class I	Address bus
L3	DDR3B_A2	AA29	1.5-V SSTL Class I	Address bus

Table 2–30. DDR3B Device Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 4)

Board Reference	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
K2	DDR3B_A3	W29	1.5-V SSTL Class I	Address bus
L8	DDR3B_A4	U23	1.5-V SSTL Class I	Address bus
L2	DDR3B_A5	AA30	1.5-V SSTL Class I	Address bus
M8	DDR3B_A6	R23	1.5-V SSTL Class I	Address bus
M2	DDR3B_A7	AC30	1.5-V SSTL Class I	Address bus
N8	DDR3B_A8	T23	1.5-V SSTL Class I	Address bus
M3	DDR3B_A9	AB29	1.5-V SSTL Class I	Address bus
H7	DDR3B_A10	R30	1.5-V SSTL Class I	Address bus
M7	DDR3B_A11	R26	1.5-V SSTL Class I	Address bus
K7	DDR3B_A12	T25	1.5-V SSTL Class I	Address bus
N3	DDR3B_A13	AD29	1.5-V SSTL Class I	Address bus
J2	DDR3B_BA0	W30	1.5-V SSTL Class I	Bank address bus
K8	DDR3B_BA1	T24	1.5-V SSTL Class I	Bank address bus
J3	DDR3B_BA2	V30	1.5-V SSTL Class I	Bank address bus
G3	DDR3B_CASN	T30	1.5-V SSTL Class I	Row address select
G9	DDR3B_CKE	L28	1.5-V SSTL Class I	Column address select
G7	DDR3B_CLK_N	P22	1.5-V SSTL Class I	Differential output clock
F7	DDR3B_CLK_P	P23	1.5-V SSTL Class I	Differential output clock
H2	DDR3B_CSN	U29	1.5-V SSTL Class I	Chip select
B7	DDR3B_DM4	P29	1.5-V SSTL Class I	Write mask byte lane
B3	DDR3B_DQ32	P28	1.5-V SSTL Class I	Data bus byte lane 4
C7	DDR3B_DQ33	K28	1.5-V SSTL Class I	Data bus byte lane 4
C2	DDR3B_DQ34	M27	1.5-V SSTL Class I	Data bus byte lane 4
C8	DDR3B_DQ35	P30	1.5-V SSTL Class I	Data bus byte lane 4
E3	DDR3B_DQ36	N29	1.5-V SSTL Class I	Data bus byte lane 4
E8	DDR3B_DQ37	M29	1.5-V SSTL Class I	Data bus byte lane 4
D2	DDR3B_DQ38	R27	1.5-V SSTL Class I	Data bus byte lane 4
E7	DDR3B_DQ39	N30	1.5-V SSTL Class I	Data bus byte lane 4
D3	DDR3B_DQS_N4	R25	Differential 1.5-V SSTL Class I	Data strobe P byte lane 4
C3	DDR3B_DQS_P4	P25	Differential 1.5-V SSTL Class I	Data strobe N byte lane 4
G1	DDR3B_ODT	V29	1.5-V SSTL Class I	On-die termination enable
F3	DDR3B_RASN	T29	1.5-V SSTL Class I	Row address select
N2	DDR3B_RESETN	AB27	1.5-V SSTL Class I	Reset
H3	DDR3B_WEN	T28	1.5-V SSTL Class I	Write enable
H8	DDR3B_ZQ05	—	1.5-V SSTL Class I	ZQ impedance calibration

Synchronous SRAM

The development board supports a 18-MB standard synchronous SRAM for instruction and data storage with low-latency random access capability. The device has a 1024K x 18-bits interface. This device is part of the shared FSM bus that connects to the flash memory, SRAM, and MAX V CPLD 5M2210 System Controller.

The device speed is 200 MHz single-data-rate. There is no minimum speed for this device. The theoretical bandwidth of this interface is 3.2 Gbps for continuous bursts. The read latency for any address is two clocks while the write latency is one clock.

Table 2–31 lists the SSRAM pin assignments, signal names, and functions.

Table 2–31. SSRAM Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 2)

Board Reference (U37)	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
86	FLASH_OEN	M8	2.5-V	Output enable
87	FLASH_WEN	J15	2.5-V	Write enable
37	FSM_A1	N10	2.5-V	Address bus
36	FSM_A2	N9	2.5-V	Address bus
44	FSM_A3	M12	2.5-V	Address bus
42	FSM_A4	M11	2.5-V	Address bus
34	FSM_A5	G7	2.5-V	Address bus
47	FSM_A6	G8	2.5-V	Address bus
43	FSM_A7	F6	2.5-V	Address bus
46	FSM_A8	G6	2.5-V	Address bus
45	FSM_A9	J10	2.5-V	Address bus
35	FSM_A10	K10	2.5-V	Address bus
32	FSM_A11	E6	2.5-V	Address bus
33	FSM_A12	E7	2.5-V	Address bus
50	FSM_A13	D6	2.5-V	Address bus
48	FSM_A14	D7	2.5-V	Address bus
100	FSM_A15	A2	2.5-V	Address bus
99	FSM_A16	A3	2.5-V	Address bus
82	FSM_A17	D8	2.5-V	Address bus
80	FSM_A18	E8	2.5-V	Address bus
49	FSM_A19	F8	2.5-V	Address bus
81	FSM_A20	G9	2.5-V	Address bus
39	FSM_A21	H9	2.5-V	Address bus
58	FSM_D0	E13	2.5-V	Data bus
59	FSM_D1	F13	2.5-V	Data bus
62	FSM_D2	C6	2.5-V	Data bus
63	FSM_D3	C7	2.5-V	Data bus
68	FSM_D4	A6	2.5-V	Data bus
69	FSM_D5	B6	2.5-V	Data bus

Table 2–31. SSRAM Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 2)

Board Reference (U37)	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
72	FSM_D6	A8	2.5-V	Data bus
73	FSM_D7	B7	2.5-V	Data bus
23	FSM_D8	B8	2.5-V	Data bus
22	FSM_D9	C9	2.5-V	Data bus
19	FSM_D10	A9	2.5-V	Data bus
18	FSM_D11	A10	2.5-V	Data bus
12	FSM_D12	C10	2.5-V	Data bus
13	FSM_D13	D9	2.5-V	Data bus
8	FSM_D14	A11	2.5-V	Data bus
9	FSM_D15	B11	2.5-V	Data bus
85	SRAM_ADSCN	P12	2.5-V	Address status controller
84	SRAM_ADSPN	J13	2.5-V	Address status processor
83	SRAM_ADVN	K13	2.5-V	Adress valid
93	SRAM_BWAN	P10	2.5-V	Byte write select
94	SRAM_BWBN	N11	2.5-V	Byte write select
97	SRAM_CE2	—	2.5-V	Chip enable 2
92	SRAM_CE3N	—	2.5-V	Chip enable 3
98	SRAM_CEN	K11	2.5-V	Chip enable 1
89	SRAM_CLK	N12	2.5-V	Clock
88	SRAM_GWN	—	2.5-V	Global write enable
31	SRAM_MODE	—	2.5-V	Burst sequence selection
64	SRAM_ZZ	—	2.5-V	Power sleep mode

Flash

The development board supports a 512-MB CFI-compatible synchronous flash device for non-volatile storage of FPGA configuration data, board information, test application data, and user code space. This device is part of the shared FSM bus that connects to the flash memory, SSRAM, and MAX V CPLD 5M2210 System Controller.

This 16-bit data memory interface can sustain burst read operations at up to 52 MHz for a throughput of 832 Mbps per device. The write performance is 270 µs for a single word buffer while the erase time is 800 ms for a 128 K array block.

Table 2–32 lists the flash pin assignments, signal names, and functions. The signal names and types are relative to the Cyclone V GX in terms of I/O setting and direction.

Table 2–32. Flash Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 3)

Board Reference (U18)	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
F6	FLASH_ADVN	H15	2.5-V	Address valid
B4	FLASH_CEN	L10	2.5-V	Chip enable

Table 2–32. Flash Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 3)

Board Reference (U18)	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
E6	FLASH_CLK	M9	2.5-V	Clock
F8	FLASH_OEN	M8	2.5-V	Output enable
F7	FLASH_RDYBSYN	L11	2.5-V	Ready
D4	FLASH_RESETN	L9	2.5-V	Reset
G8	FLASH_WEN	J15	2.5-V	Write enable
C6	FLASH_WPN	—	2.5-V	Write protect
A1	FSM_A1	N10	2.5-V	Address bus
B1	FSM_A2	N9	2.5-V	Address bus
C1	FSM_A3	M12	2.5-V	Address bus
D1	FSM_A4	M11	2.5-V	Address bus
D2	FSM_A5	G7	2.5-V	Address bus
A2	FSM_A6	G8	2.5-V	Address bus
C2	FSM_A7	F6	2.5-V	Address bus
A3	FSM_A8	G6	2.5-V	Address bus
B3	FSM_A9	J10	2.5-V	Address bus
C3	FSM_A10	K10	2.5-V	Address bus
D3	FSM_A11	E6	2.5-V	Address bus
C4	FSM_A12	E7	2.5-V	Address bus
A5	FSM_A13	D6	2.5-V	Address bus
B5	FSM_A14	D7	2.5-V	Address bus
C5	FSM_A15	A2	2.5-V	Address bus
D7	FSM_A16	A3	2.5-V	Address bus
D8	FSM_A17	D8	2.5-V	Address bus
A7	FSM_A18	E8	2.5-V	Address bus
B7	FSM_A19	F8	2.5-V	Address bus
C7	FSM_A20	G9	2.5-V	Address bus
C8	FSM_A21	H9	2.5-V	Address bus
A8	FSM_A22	J9	2.5-V	Address bus
G1	FSM_A23	H7	2.5-V	Address bus
H8	FSM_A24	J7	2.5-V	Address bus
B6	FSM_A25	A4	2.5-V	Address bus
B8	FSM_A26	A5	2.5-V	Address bus
F2	FSM_D0	E13	2.5-V	Data bus
E2	FSM_D1	F13	2.5-V	Data bus
G3	FSM_D2	C6	2.5-V	Data bus
E4	FSM_D3	C7	2.5-V	Data bus
E5	FSM_D4	A6	2.5-V	Data bus
G5	FSM_D5	B6	2.5-V	Data bus
G6	FSM_D6	A8	2.5-V	Data bus

Table 2–32. Flash Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 3)

Board Reference (U18)	Schematic Signal Name	Cyclone V GX Pin Number	I/O Standard	Description
H7	FSM_D7	B7	2.5-V	Data bus
E1	FSM_D8	B8	2.5-V	Data bus
E3	FSM_D9	C9	2.5-V	Data bus
F3	FSM_D10	A9	2.5-V	Data bus
F4	FSM_D11	A10	2.5-V	Data bus
F5	FSM_D12	C10	2.5-V	Data bus
H5	FSM_D13	D9	2.5-V	Data bus
G7	FSM_D14	A11	2.5-V	Data bus
E7	FSM_D15	B11	2.5-V	Data bus

Power Supply

You can power up the development board either from a laptop-style DC power input or from the PCI Express edge connector. The input voltage must be in the range of 14 V to 20 V. The DC voltage is then stepped down to various power rails used by the board components and installed into the HSMC connectors.

Table 2–33 outlines the allowable power inputs.

Table 2–33. Power Inputs

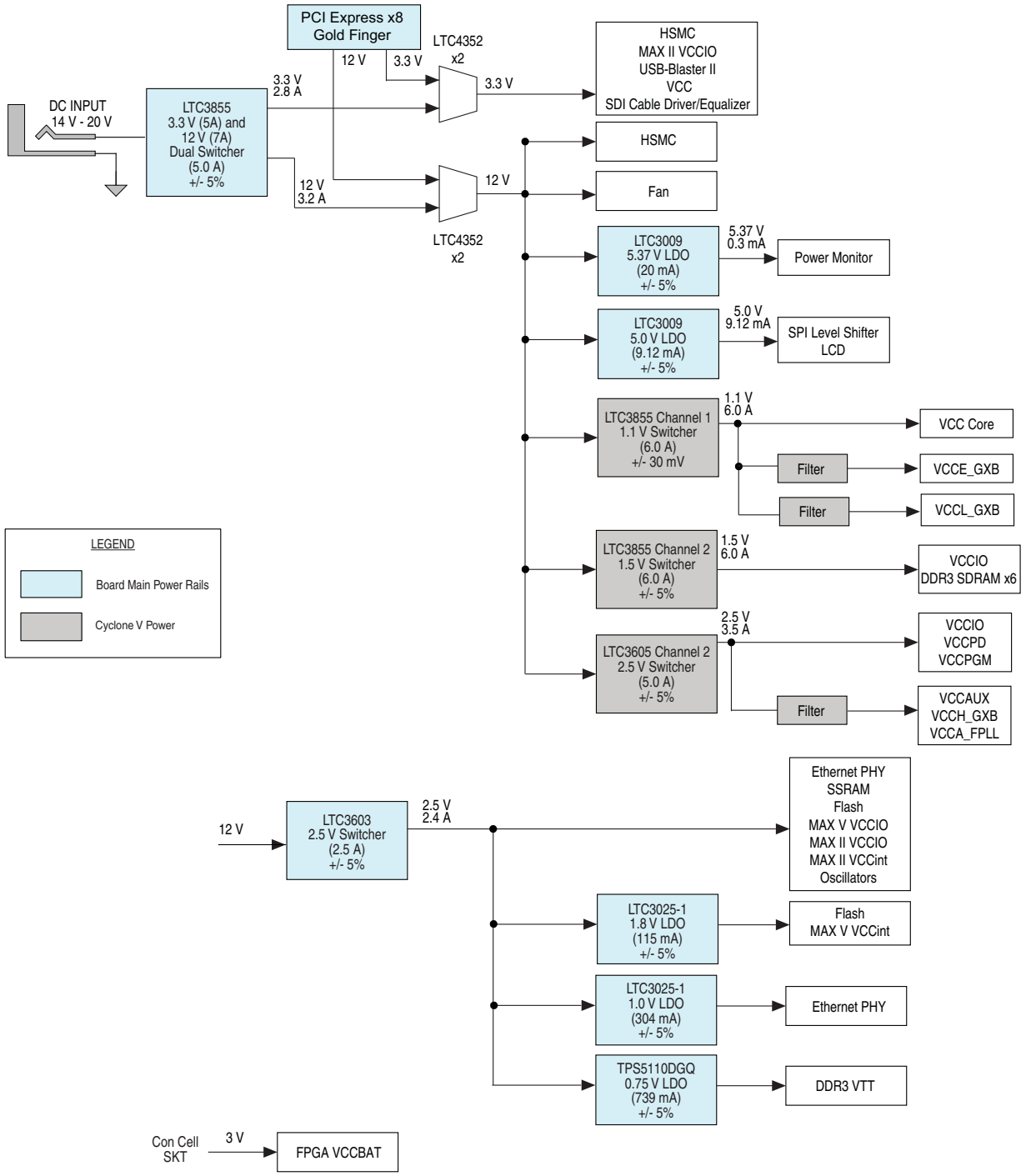
Power Source	Voltage (V)	Current (A)	Maximum Wattage (W)
Laptop-style DC input	15.0	4.3	65
25-W PCI Express edge connector	3.3	3.0	9
	12.0	2.1	16
75-W PCI Express edge connector	3.3	3.0	9
	12.0	5.5	66

An on-board multi-channel analog-to-digital converter (ADC) measures the current for several specific board rails.

Power Distribution System

Figure 2–10 shows the power distribution system on the development board. Regulator inefficiencies and sharing are reflected in the currents shown, which are conservative absolute maximum levels.

Figure 2–10. Power Distribution System



Power Measurement

There are eight power supply rails that have on-board current sense capabilities using 24-bit differential ADC devices. Precision sense resistors split the ADC devices and rails from the primary supply plane for the ADC to measure current. A SPI bus connects these ADC devices to the MAX V CPLD 5M2210 System Controller.

Figure 2–11 shows the block diagram for the power measurement circuitry.

Figure 2–11. Power Measurement Circuit

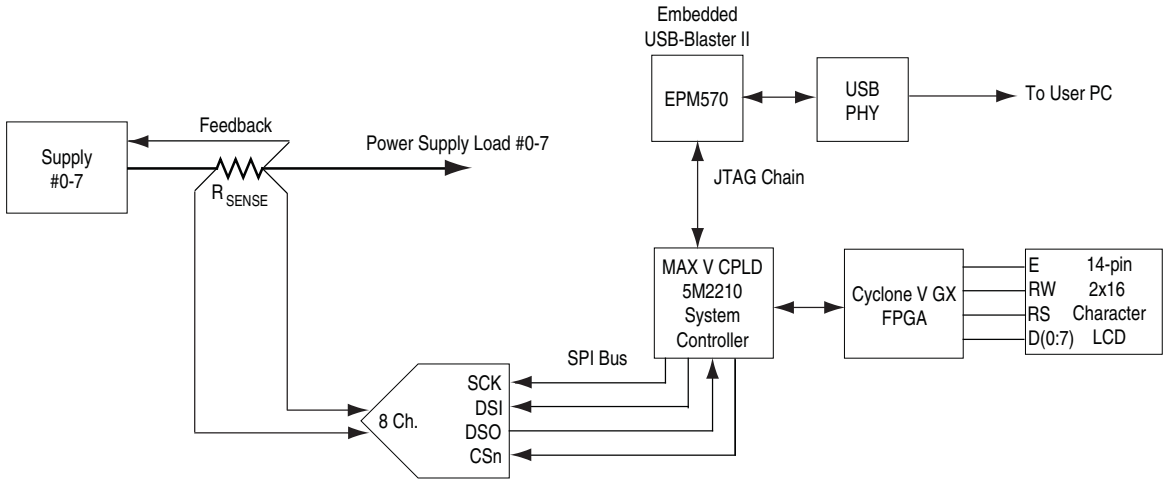


Table 2–34 lists the targeted rails. The schematic signal name column specifies the name of the rail being measured while the device pin column specifies the devices attached to the rail.

Table 2–34. Power Measurement Rails

Channel	Schematic Signal Name	Voltage (V)	Device Pin	Description
1	C5_VCC_VCCE_GXB_VCCL_GXB	1.1	VCC	FPGA core and periphery power
		1.1	VCCE_GXB	XCVR analog transmit
		1.1	VCCL_GXB	XCVR analog clock network
2	C5_VCCAUX_VCCA_FPLL	2.5	VCCA_FPLL	PLL analog power
		2.5	VCC_AUX	Auxiliary
3	C5_VCCIO_VCCPD_PGM	2.5	VCCPD	I/O pre-drivers
		2.5	VCCPGM	Configuration I/O
		2.5	VCCIO_3A, VCCIO_5A, VCCIO_7A, VCCIO_8A	VCC I/O banks 3, 7, and 8
4	C5_VCCIO_1.5V	1.5	VCCIO_6A, VCCIO_5B, VCCIO_4A, VCCIO_3B	VCCIO bank (DDR3)
5	C5_VCCBAT	3.0	VCCBAT	Battery power
6	C5_VCCH_GXBL	2.5	VCCH_GXB	XCVR block level transmit buffers

Statement of China-RoHS Compliance

Table 2–35 lists hazardous substances included with the kit.

Table 2–35. Table of Hazardous Substances' Name and Concentration *Notes* (1), (2)

Part Name	Lead (Pb)	Cadmium (Cd)	Hexavalent Chromium (Cr6+)	Mercury (Hg)	Polybrominated biphenyls (PBB)	Polybrominated diphenyl Ethers (PBDE)
Cyclone V GX development board	X*	0	0	0	0	0
15 V power supply	0	0	0	0	0	0
Type A-B USB cable	0	0	0	0	0	0
User guide	0	0	0	0	0	0

Notes to Table 2–35:

(1) 0 indicates that the concentration of the hazardous substance in all homogeneous materials in the parts is below the relevant threshold of the SJ/T11363-2006 standard.

(2) X* indicates that the concentration of the hazardous substance of at least one of all homogeneous materials in the parts is above the relevant threshold of the SJ/T11363-2006 standard, but it is exempted by EU RoHS.

3. Board Components Reference

This chapter lists the component reference and manufacturing information of all the components on the Cyclone V GX FPGA development board.

Table 3–1. Component Reference and Manufacturing Information

Board Reference	Component	Manufacturer	Manufacturing Part Number	Manufacturer Website
U11	FPGA, Cyclone V GX F1152, 150K LEs, leadfree	Altera Corporation	5CGXFC7D6F31C7NES	www.altera.com
U12	MAX V CPLD 5M2210 System Controller	Altera Corporation	5M2210ZF256C4N	www.altera.com
U16	High-Speed USB peripheral controller	Cypress	CY7C68013A	www.cypress.com
D1–D7, D12–D15, D17–D22, D24–D28	Green LED	Lumex Inc.	SML-LXT0805GW-TR	www.lumex.com
D8–D10	Yellow LED	Lumex Inc.	SML-LXT0805SYW-TR	www.lumex.com
D16	Red LED	Lumex Inc.	SML-LXT0805IW-TR	www.lumex.com
D23	Blue LED	Lumex Inc.	SML-LX0805USBC-TR	www.lumex.com
SW2–SW5	Four-position DIP switch	C&K Components/ ITT Industries	TDA04H0SB1	www.ittcannon.com
S1, S4, S6, S7	Push button	Panasonic	EVQPAC07K	www.panasonic.com
S3–S5	Push button	Dawning Precision Co.	TS-A02SA-2-S100	www.dawning2.com.tw
U25	Programmable LVDS quad-clock 125M, 409.6M, 156.25M, 100M defaults	Silicon Labs	Si5338A-A01343-GM	www.silabs.com
X2	148.50 MHz LVDS voltage controlled crystal oscillator	Silicon Labs	571FDB000159DG	www.silabs.com
X1	100 MHz crystal oscillator, ±50 ppm, CMOS, 2.5 V	Silicon Labs	510GBA100M000BAGx	www.silabs.com
X4	50 MHz crystal oscillator, ±50 ppm, CMOS, 2.5 V	Silicon Labs	510GBA50M0000BAGx	www.silabs.com
J18	2×7 pin LCD socket strip	Samtec	TSM-107-07-G-D	www.samtec.com
	2×16 character LCD, 5×8 dot matrix	Lumex Inc.	LCM-S01602DSR/C	www.lumex.com
U10	Ethernet PHY BASE-T device	Marvell Semiconductor	88E1111-B2-CAA1C000	www.marvell.com
J11	RJ-45 connector, 10/100/1000 Mbps	Wurth Elektronik	7499111001A	www.we-online.com
J1	HSMC, custom version of QSH-DP family high-speed socket.	Samtec	ASP-122953-01	www.samtec.com
U1	3-Gbps HD/SD SDI cable driver with cable detect	National Semiconductor	LMH0303SQx	www.national.com

Table 3–1. Component Reference and Manufacturing Information

Board Reference	Component	Manufacturer	Manufacturing Part Number	Manufacturer Website
U4	3-Gbps HD/SD SDI adaptive cable equalizer	National Semiconductor	LMH0384SQ	www.national.com
J14	2x7 debug header	Samtec	TSW-107-07	www.samtec.com
U6, U15, U21, U22	16M×16×8, 128-MB DDR3 SDRAM	Micron	MT41J128M16	www.micron.com
U19, U23	16M×8×8, 128-MB DDR3 SDRAM	Micron	MT41J128M8	www.micron.com
U37	1024K×18 bit 18-MB synchronous SRAM	Integrated Silicon Solution, Inc.	IS61VPS102418A-250TQL	www.issi.com
U18	512-MB synchronous flash	Numonyx	PC28F512P30BF	www.numonyx.com
U17	16-channel differential 24-bit ADC	Linear Technology	LTC2418CGN#PBF	www.linear.com

This chapter provides additional information about the document and Altera.

Document Revision History

The following table lists the revision history for this document.

Date	Version	Changes
May 2013	1.2	■ Revised the device part number to 5CGXFC7D6F31C7NES.
October 2012	1.1	■ Revised the default settings in Table 2–8 and Table 2–9. ■ Updated the device pin numbers in Table 2–26 and Table 2–28. ■ Revised the power inputs in Table 2–33. ■ Updated Figure 2–4.
September 2012	1.0	Initial release.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact (1)	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Nontechnical support (general)	Email	nacomp@altera.com
(software licensing)	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, **Save As** dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, **\qdesigns** directory, **D:** drive, and **chiptrip.gdf** file.

Visual Cue	Meaning
Italic Type with Initial Capital Letters	Indicate document titles. For example, *Stratix IV Design Guidelines*.
italic type	Indicates variables. For example, *n* + 1. Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>*.**pof** file.
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, "Typographic Conventions."
`Courier type`	Indicates signal, port, register, bit, block, and primitive names. For example, `data1`, `tdi`, and `input`. The suffix `n` denotes an active-low signal. For example, `resetn`. Indicates command line commands and anything that must be typed exactly as it appears. For example, `c:\qdesigns\tutorial\chiptrip.gdf`. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), and logic function names (for example, `TRI`).
↵	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■ ■	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	The question mark directs you to a software help system with related information.
	The feet direct you to another document or website with related information.
	The multimedia icon directs you to a related multimedia presentation.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.
	The feedback icon allows you to submit feedback to Altera about the document. Methods for collecting feedback vary as appropriate for each document.